SSD1502 Display Driver

for

The CyberDisplay® VGA Color Display

Part Numbers:
KCD-A900-QA (TQFP80 package)
KCD-A900-QA-TP (BGA80 package)

Ver. 0.1
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KOPIN

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1 General Description

SSD1502 is a highly integrated controller solution to *KOPIN CyberDisplay® VGA VGA microdisplay*, together with the analog driver. It includes all the timing control, image processing, buffer control, data transaction units, a scaling buffer memory, and three 8-bit DACs. It provides a low power timing control signal for the analog chip and employs a gated-clock ASIC design to achieve a low power solution.

The controller chip supports digital input formats. Digital inputs are formatted by the Horizontal and Vertical Scaling block to achieve 640x480 output pixels. There is YCbCr to RGB conversion block and a Gamma Correction block for add on data processing. Three 8-bit DACs convert 8-bit digital video data to 1Vpp analog video signal. It generates digital control signals and analog video data to the microdisplay and analog chip.

2 FEATURES

- Support TV-Decoder image inputs using CCIR601 format or digital VESA VGA with separate sync
- Compatible video decoders include Philips SAA7111A and SAA7113
- Digital input formats:
  - NTSC and PAL video (support rectangle and square pixel variants)
  - BT656, with sync information in SAV/EAV blocks (8-bit words @ 27MHz)
  - 4:2:2 YCbCr (8-bit words @ 27MHz or 16-bit words @ 13.5MHz)
  - 16-bit RGB (5,6,5) @ 13.5 MHz
  - VESA VGA video
  - 480p RGB/YCbCr with separate sync signals which Hsync, Vsync and Pixel clock (Pclk) (24-bit words @ 25-36MHz).
  - Serial wire interface for YCbCr video input source
- NTSC/PAL and VESA VGA resolution
- Flexible Horizontal and Vertical scaling
- Programmable 9 entries gamma correction
- I^2C interface
- NTSC and PAL Deinterlace
- Embedded line buffer for scaling
- Triple integrated 8-bit DAC
- Programmable control of PWM color backlight flash timing with external pin to control duty cycle
- Programmable timing control of CyberDisplay VGA display.
- Core and I/O 3.3V operating voltage
- Stereo Video support
- TQFP and BGA package available

3 ORDERING INFORMATION

Ordering Part Number	Package Form
KCD-A900-QA	TQFP80
KCD-A900-QA-TP	BGA80

Table 1: Ordering Information

4 BLOCK DIAGRAM

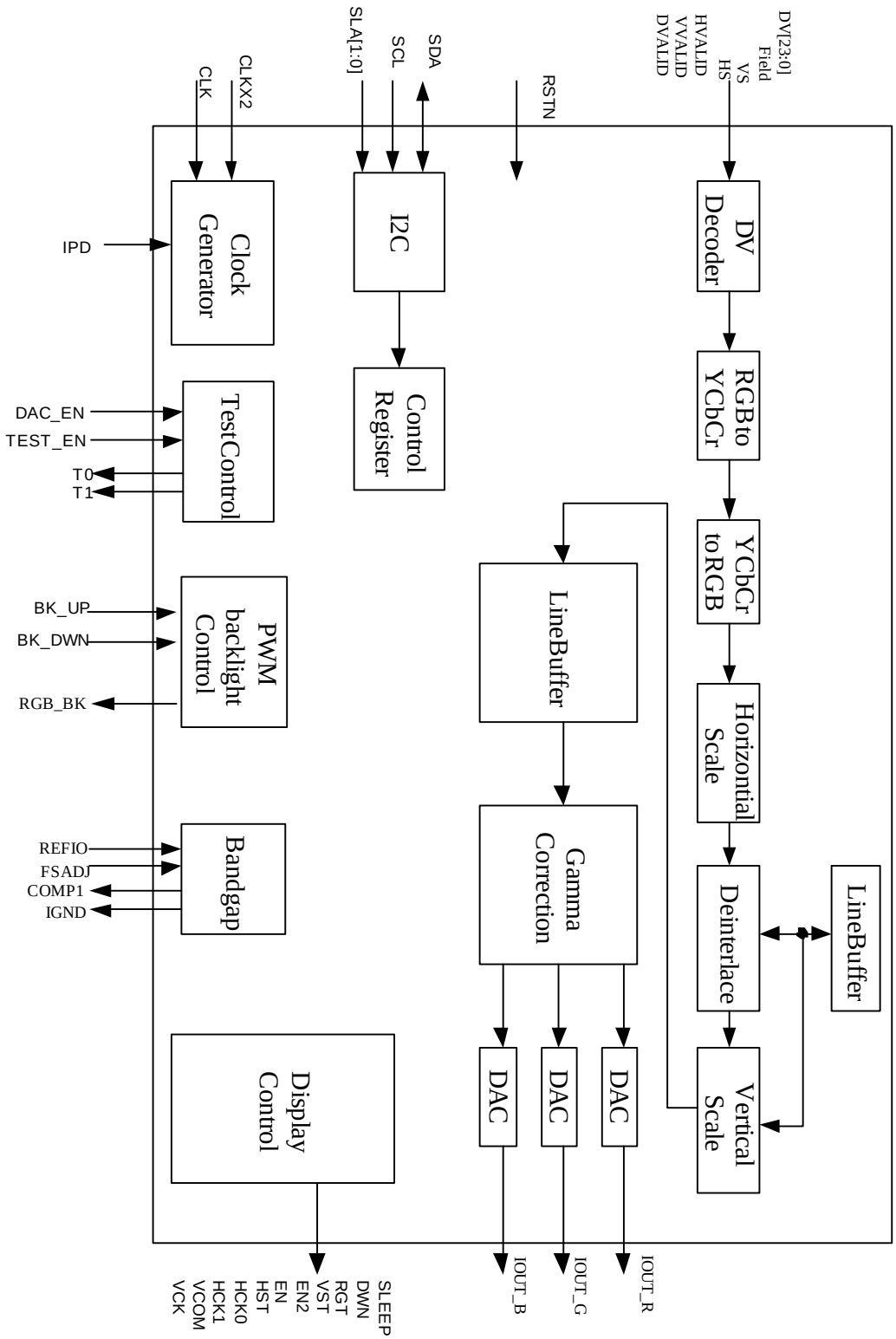


Figure 1: SSD1502 Block Diagram

5 PIN DESCRIPTION

Table 2: Pin Description

TQFP pin no.	BGA pin no.	Name	Direction	Pin Description
1	J1	DV23	I	Digital video input
2	H2	DV22	I	Digital video input
3	G3	DV21	I	Digital video input
4	F4	RSTN	I	System reset
5	J2	CLKX2	I	External 2X clock input
6	H3	CLK	I	External clock input
7	G4	DV20	I	Digital video input
8	F5	DV19	I	Digital video input
9	J3	DV18	I	Digital video input
10	H4	DV17	I	Digital video input
11	G5	T1	O	Test output signal 1
12	J4	DVSS	P	Digital VSS power
13	H5	DVDD	P	Digital VDD power
14	G6	BK_DWN	I	Backlight PWM duty down
15	J5	BK_UP	I	Backlight PWM duty up
16	H6	BK_RGB	O	Backlight Control
17	J6	SDA	I/O	Serial data input/output for I2C bus
18	H7	SCL	I	Serial clock input for I2C bus
19	J7	SLA1	I	I2C slave address setting
20	J8	SLA0	I	I2C slave address setting
21	J9	IPD	I	External Power Down Control. VDD for power down. VSS for Normal
22	H8	NC	-	-
23	G7	SLEEP	O	Sleep Mode
24	F6	DWN	O	Top-to-bottom scan
25	H9	RGT	O	Left-to-right scan
26	G8	VST	O	Vertical start pulse
27	F7	EN2	O	Row Enable for Field stereo panel 2
28	E6	EN	O	Row Enable
29	G9	HST	O	Horizontal start pulse
30	F8	HCK0	O	Horizontal clock 0
31	E7	HCK1	O	Horizontal clock 1
32	F9	DVDD	P	Digital VDD power
33	E8	DVSS	P	Digital VSS power
34	D7	TEST1	I	Internal test pin, connect to ground by default
35	E9	TEST2	I	Internal test pin, connect to ground by default
36	D8	VCOM	O	Common ITO electrode
37	D9	VCK	O	Vertical clock
38	C8	NC	-	-
39	C9	NC	-	-
40	B9	NC	-	-

TQFP pin no.	BGA pin no.	Name	Direction	Pin Description
41	A9	AVSS	P	Analog VSS power
42	B8	AVDD	P	Analog VDD power
43	C7	IOUTB	AO	DAC current output port for blue video output
44	D6	IOUTG	AO	DAC current output port for green video output
45	A8	IGND	AO	Current Ground. Connect to AVSS for normal operation
46	B7	IOUTR	AO	DAC current output port for red video output
47	C6	COMP1	AO	Bandwidth/noise reduction node. Add 0.1 uF to AVSS for optimum performance
48	D5	FSADJ	AI	DAC Full-scale current output adjustment. Add an external resistor between this pin and AVSS
49	A7	REFIO	AI	Bandgap Input Voltage Reference.
50	B6	NC	-	-
51	C5	DVDD	P	Digital VDD power
52	A6	DVSS	P	Digital VSS power
53	B5	TEST3	I	Internal test pin, connect to ground by default
54	C4	TEST4	I	Internal test pin, connect to ground by default
55	A5	T2	O	Test output signal 2
56	B4	FIELD	I	Field input signal
57	A4	DV7	I	Digital video input
58	B3	DV6	I	Digital video input
59	A3	DV5	I	Digital video input
60	A2	DV4	I	Digital video input
61	A1	DV3	I	Digital video input
62	B2	DV2	I	Digital video input
63	C3	DV1	I	Digital video input
64	D4	DV0	I	Digital video input
65	B1	DV15	I	Digital video input
66	C2	DV14	I	Digital video input
67	D3	DV13	I	Digital video input
68	E4	DV12	I	Digital video input
69	C1	DV11	I	Digital video input
70	D2	DV10	I	Digital video input
71	E3	DV9	I	Digital video input
72	D1	DV8	I	Digital video input
73	E2	DVSS	P	Digital VSS power
74	F3	DVDD	P	Digital VDD power
75	E1	HVALID	I	Horizontal valid input signal
76	F2	VVALID	I	Vertical valid input signal
77	F1	DVALID	I	Data Valid input signal
78	G2	HS	I	Horizontal sync input signal
79	G1	VS	I	Vertical sync input signal
80	H1	DV16	I	Digital video input

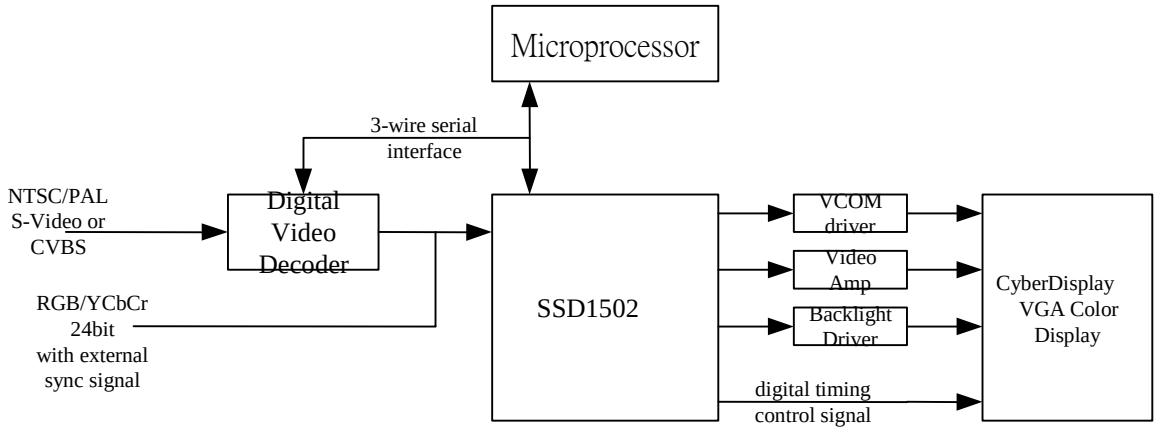
Pin Type Description

I – digital input pad;
O –digital output pad;
I/O – digital bi-directional pad;
AI – analog input;
AO – analog output;
P – Power pad

6 FUNCTIONAL BLOCK DESCRIPTIONS

The SSD1502 converts standard digital video for the Kopin CyberDisplay™ VGA display. A typical system block diagram is shown below. The SSD1502 provides all necessary digital control signals to the display. Integrated DAC output analog video signals to the external amplifiers.

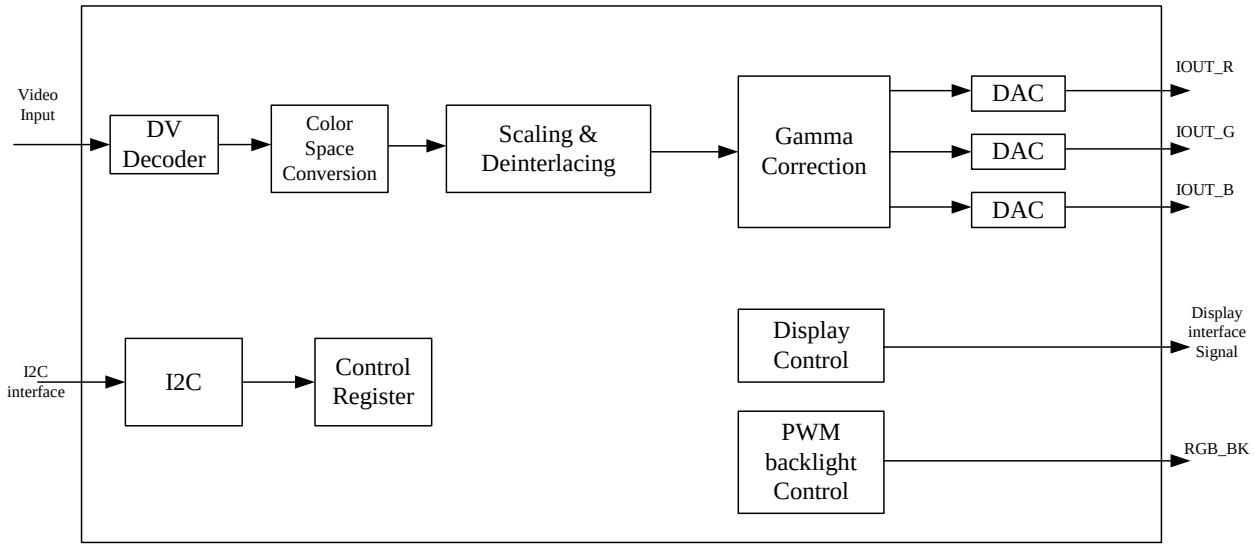
Figure 2: System Block Diagram



The SSD1502 accepts digital video signals directly, or an external decoder may be used for analog video inputs. The I^2C bus is used to program both the decoder and the SSD1502.

Figure 3 shows the functional blocks within the SSD1502, each of which is discussed below.

Figure 3: Functional Block Diagram



6.1 Deinterlace

For NTSC/PAL video input requires deinterlacing to enhance the image quality. The purpose scheme is as following:

1. Double Line Buffer
2. Median Filter

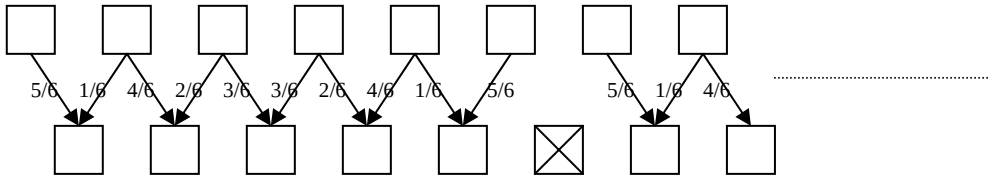
6.2 Scaling

After the digital video decoder, the line will be discarded as the standard format. Table 3 shows the standard NTSC/PAL format. Each line output by the digital video interface contains 640 RGB samples. A 9:8 and 6:5 scaling operation is required to fit the display resolution from 720 to 640 columns and 768 to 640 columns. The horizontal scale also provides 11:10 scaling to perform. Each line with 720 pixels is cropped 8 pixels at both the front and back of each line and then performs 11:10 scaling to fit 640 pixel sizes. Figure 4 illustrates the decimation algorithm of 6:5, in which each output pixel is the weighted average of two input pixels. Other scaling is performed with a similar algorithm.

Table 3: Standard NTSC and PAL format

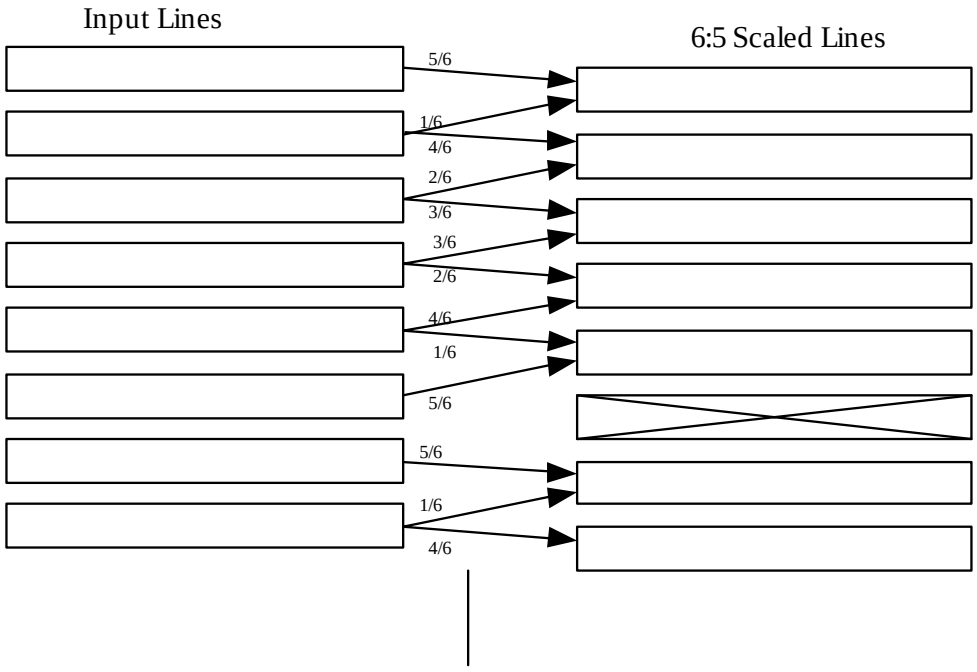
Format	Horizontal Pixel Size	Vertical Size
Rectangle NTSC	720	480
Rectangle PAL	720	576
Square NTSC	640	480
Square PAL	768	576

Figure 4: Horizontal Scaling (6:5)



The NTSC format has 480 valid lines in the odd and even fields after deinterlacing. However, the PAL format requires 6:5 vertical scaling to fit 576 input lines into 480 display lines. The algorithm of the vertical scale is similar to that used in the horizontal case. The vertical scaler is automatically bypassed when the NTSC input video format is used.

Figure 5: Vertical Scaling (6:5)



6.3 Gamma Correction

The SSD1502 features a programmable gamma correction feature to compensate for the display's non-linear electro-optical response. A 9-entry lookup table (LUT) specifies a piecewise-linear function. Intermediate values are interpolated from the nearest LUT entries.

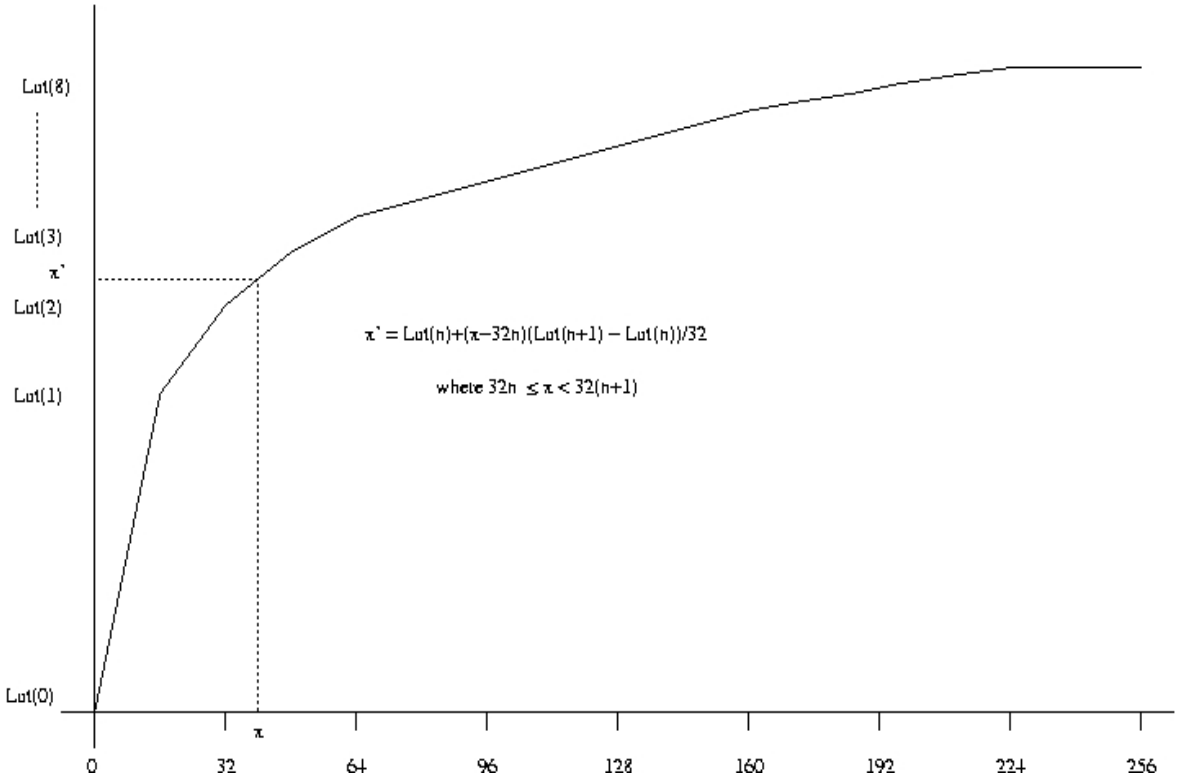


Figure 6: Piecewise-linear Gamma Function

6.3 Display Controller

The display controller block generates the necessary control signals for the CyberDisplay™ VGA display. The timing is derived from that of the external video source. Both NTSC and PAL video formats are supported. LED backlight timing is programmable to adjust color balance and uniformity by Pulse Width Modulation (PWM).

6.5 Backlight Controller

Backlight output is controlled by Pulse Width Modulation (PWM) controller. This duty cycle and clock period of backlight can be configured through the control register. The block diagram of the PWM Controller and the Backlight Output Timing Diagram are shown below.

Figure 7: Backlight output timing diagram

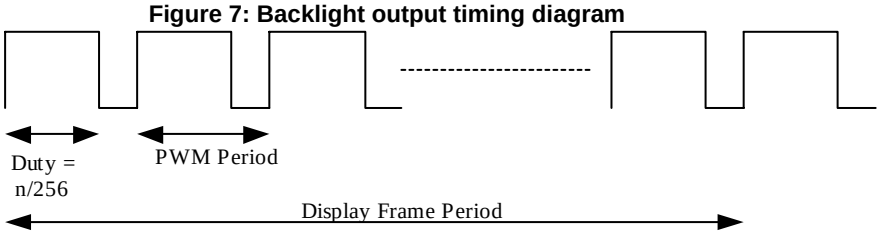
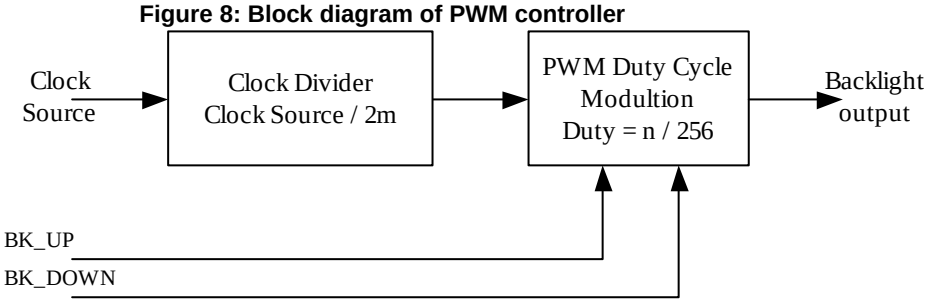


Figure 8: Block diagram of PWM controller



The PWM Duty Cycle can be controlled I^2C and 2 external input pins BK_UP and BK_DWN. The PWM controller will sample input pins of each frame to increase or decrease one duty cycle width.

6.6 Color Space Conversion

Color space conversion will be performed, depending on the input signals. In either case, the following conversions are required:

- RGB -> RGB — Primary color signals on color display
- YCbCr -> RGB — Luminance/Chrominance signals on color display.
- Y -> RGB — Monochrome signal on color display
  RGB->Y->RGB — Color signal converted to monochrome, and shown on color display

The controller contains YCbCr to RGB conversion and RGB to YCbCr conversion features. There are enable signals to on and off one or both features. In register 0x90, monochrome bit is used to output black and white picture. CSC_Mode bit is used to select one out of three conversion standards. There are also Y_offset, Cb_offset, Cr_offset in register 0x98, 0x99 and 0x9A for color space tuning.

If YCbCr to RGB enable bit is set, the conversion equations for different CSC_Mode bit setting are listed below.

CSC_Mode = 00 (SMTPE 170M)
R = Y + 1.40200 * (Cr-128)
G = Y - 0.34414 * (Cb-128) - 0.71414 * (Cr-128)
B = Y + 1.77200 * (Cb-128)

CSC_Mode = 01 (CCIR 601)
R = Y + 1.371 * (Cr – 128)
G = Y - 0.336 * (Cb –128) - 0.698 * (Cr-128)
B = Y + 1.732 * (Cb-128)

CSC_Mode = 10 (BT601)

R = 1.164 * (Y - 16) + 1.596 * (Cr - 128)
G = 1.164 * (Y - 16) - 0.391 * (Cb - 128) - 0.813 * (Cr - 128)
B = 1.164 * (Y - 16) + 2.018 * (Cb - 128)

If RGB to YCbCr enable bit is set, the color space conversion equations become:

CSC_Mode = 00 (SMTPE 170M)
Y = 0.29891 * R + 0.58661 * G + 0.11448 * B
Cb = -0.16874 * R - 0.33126 * G + 0.50000 * B
Cr = 0.50000 * R - 0.41869 * G - 0.08131 * B

CSC_Mode = 01 (CCIR 601)
Y = 0.299 * R + 0.587 * G + 0.114 * B
Cb = -0.172 * R - 0.339 * G + 0.511 * B
Cr = 0.511 * R - 0.428 * G - 0.083 * B

CSC_Mode = 10 (BT601)
Y = 0.257 * R + 0.504 * G + 0.098 * B + 16
Cb = -0.148 * R - 0.291 * G + 0.439 * B + 128
Cr = 0.439 * R - 0.368 * G - 0.071 * B + 128

6.7 Self-test Test Pattern Controller

The SSD1502 provides self-test patterns. The SSD1502 also includes a built-in video synchronization signal generator, so that it can display test patterns in the absence of an input video signal.

6.8 Stereo Video Support

The field stereo video interleave modes write alternate fields to the left and right eyes. Full resolution is preserved, but the frame rate is halved. This stereo video mode is requires one more EN pin (EN2) to control another display panel. It supports both NTSC/PAL and VESA VGA input with external fields. The field is used field interleave to the left and right eyes. The circuit connection is as shown below. For example, if the image changes from white to black in each field alternately, the output image of the different panels would be white and black with the half frame rate only.

Figure 9: Field stereo video interleave output image

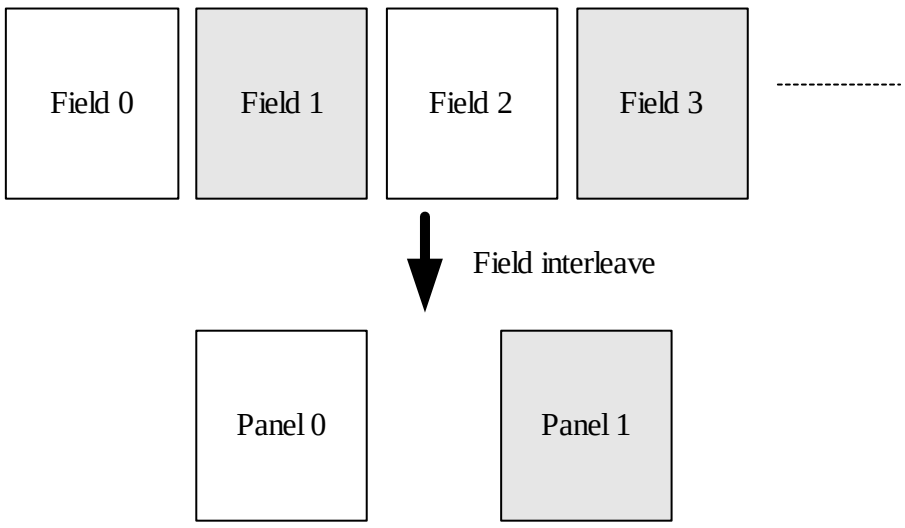
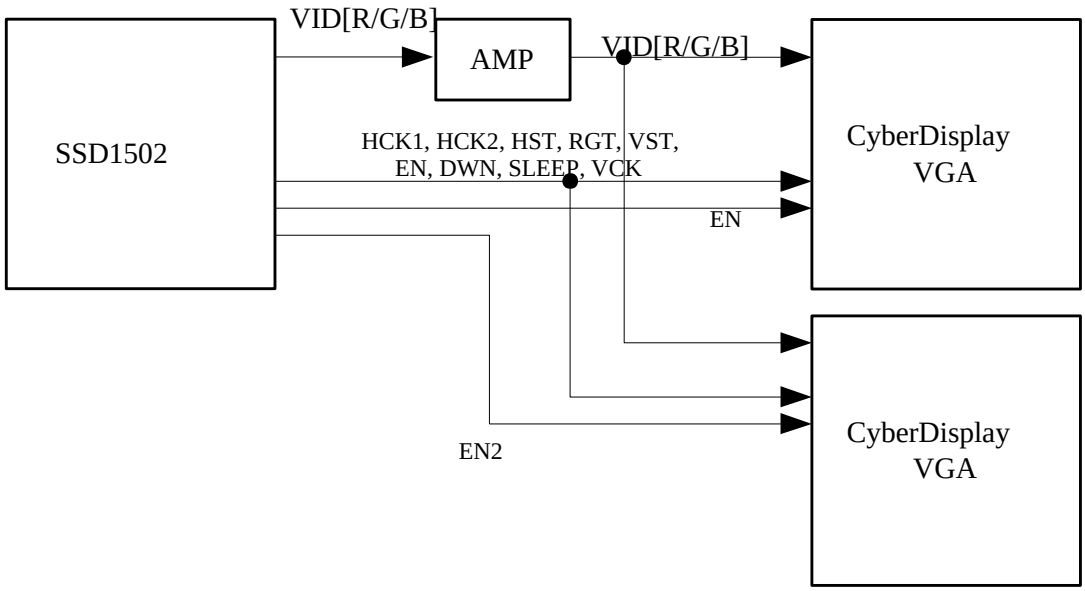


Figure 10: Progressive Input Control for Field Interleave Mode.



The line stereo video interleave mode updates both displays at the full frame rate, but cuts the vertical resolution in half. The different controllers will deinterlace in odd and even rows individually which is shown as below. Deinterlaced videos are written to the left- and right- eye displays are written individually. Because of the line interleave for each display, it can only support progressive input video signals. For example, if the rows are white and black alternately, the output of the stereo images will be white and black.

Figure 11: Line Stereo Video Interleave Output Image

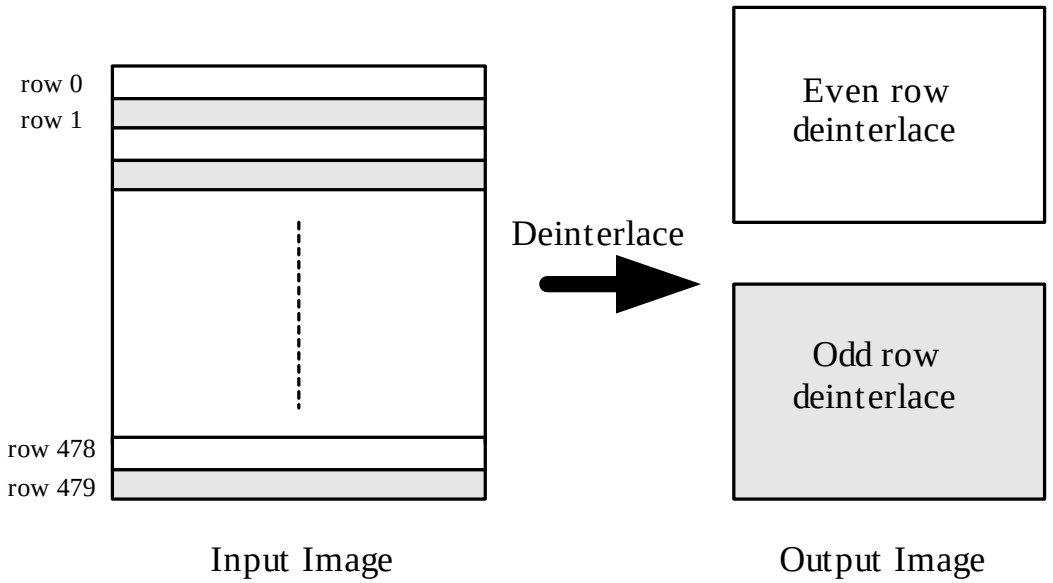
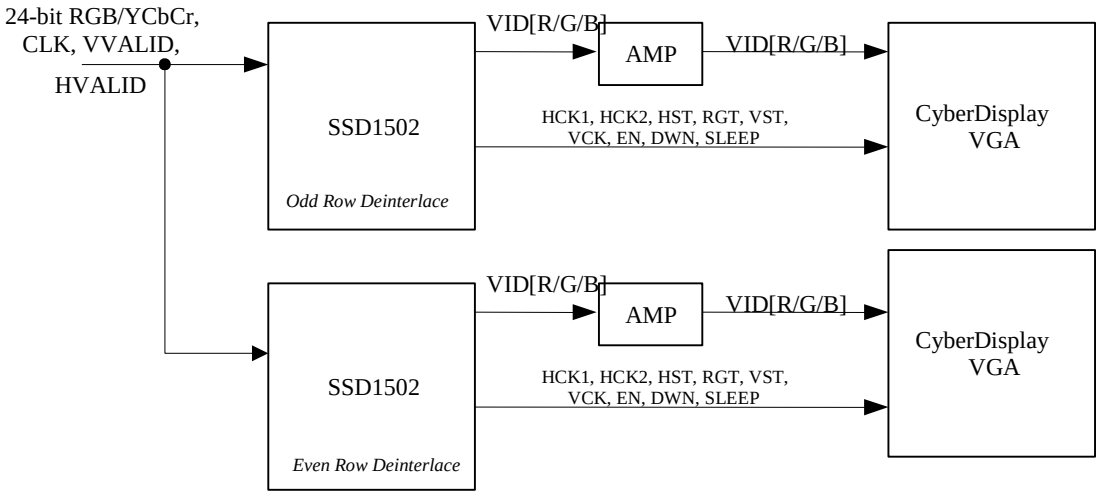


Figure 12: Progressive Input Control for Field Interleave Mode



Progressive Video Signal Input

6.9 Built-in Self-Test Memory

Embedded line memory will be tested by built-in test mode to achieve low cost and high test coverage.

6.10 I²C Interface

The I²C slave address is selectable. Pins SLA0 and SLA1 may select an alternate address (Table 4), if necessary to avoid conflicts with other devices.

Table 4: I²C Slave Address Selection

SLA1	SLA0	Slave address (hex)
0	0	68
0	1	6A
1	0	6C
1	1	6E

The SSD1502's I²C write and read formats are described below. Most writes take effect on the next vertical field, except for writes affecting video synchronization, which are effective immediately.

6.10.1 I²C Write Format

STA →SLA + Wb → ACK_S → REG_ADDR → ACK_S → DATAW1 →ACK_S → DATAW2 →·····→ DATAWn → STP

6.10.2 I²C Read Format

STA →SLA + Wb →ACK_S → REG_ADDR → ACK_S → Sr → SLA+R → DATAR1 →ACKm → DATAR2 →·····→DATARn → ACKm → STP

Or

STA →SLA + Wb →ACK_S → REG_ADDR → ACK_S → STP → STA → SLA+R → DATAR1 → ACKm → DATAR2 →·····→DATARn → ACKm → STP

Note:

STA : start condition SLA : slave address

ACKs : acknowledge from slave REG_ADDR : register address

DATAW : write data STP : stop condition
Sr : repeated start condition DATAR : read data
ACKm : acknowledge from master
REG_ADDR will auto-increment when the number of DATAW is greater than one.
REG_ADDR will auto-increment when the number of DATAR is greater than one.

6.11 Digital Video Interface

6.11.1 NTSC/PAL input signal

The digital video interface accepts CIRR.601/656 or RGB (5,6,5) video input from an external decoder or another digital video source. Not all SSD1502 data and control inputs are needed for all decoders and formats. Table 5 illustrates the signal mapping in different digital video input inteface. Table 6 summarizes the signal requirements for several decoders and formats.

Table 5: Signal Mapping in Different Digital Video Input Interface

Type	YCbCr 422		YCbCr 444	RGB 565	RGB 888	YCbCr 422				10-12 Wire Serial Mode			
Pin	2N	+1	N	N	N	4N	+1	+2	+3	4N	+1	+1	+3
DV0	Cb0	Cr0	Cb0	B0	B0					Cb0	Cb4	Cr0	Cr4
DV1	Cb1	Cr1	Cb1	B1	B1					Cb1	Cb5	Cr1	Cr5
DV2	Cb2	Cr2	Cb2	B2	B2					Cb2	Cb6	Cr2	Cr6
DV3	Cb3	Cr3	Cb3	B3	B3					Cb3	Cb7	Cr3	Cr7
DV4	Cb4	Cr4	Cb4	B4	B4								
DV5	Cb5	Cr5	Cb5	G0	B5								
DV6	Cb6	Cr6	Cb6	G1	B6								
DV7	Cb7	Cr7	Cb7	G2	B7								
DV8	Y0	Y0	Y0	G3	G0	Cb0	Y0	Cr0	Y0	Y0	Y4	Y0	Y4
DV9	Y1	Y1	Y1	G4	G1	Cb1	Y1	Cr1	Y1	Y1	Y5	Y1	Y5
DV10	Y2	Y2	Y2	G5	G2	Cb2	Y2	Cr2	Y2	Y2	Y6	Y2	Y6
DV11	Y3	Y3	Y3	R0	G3	Cb3	Y3	Cr3	Y3	Y3	Y7	Y3	Y7
DV12	Y4	Y4	Y4	R1	G4	Cb4	Y4	Cr4	Y4				
DV13	Y5	Y5	Y5	R2	G5	Cb5	Y5	Cr5	Y5				
DV14	Y6	Y6	Y6	R3	G6	Cb6	Y6	Cr6	Y6				
DV15	Y7	Y7	Y7	R4	G7	Cb7	Y7	Cr7	Y7				
DV16			Cr0		R0								
DV17			Cr1		R1								
DV18			Cr2		R2								
DV19			Cr3		R3								
DV20			Cr4		R4								
DV21			Cr5		R5								
DV22			Cr6		R6								
DV23			Cr7		R7								

Table 6: Signal Requirements for Various Decoders and Formats

Signal name	PHILIPS SAA7111 8-bit CIRR601	PHILIPS SAA7111 16-bit CIRR601	PHILIPS SAA7113 8-bit CIRR656
DV[8:15]	√	√	√
DV[0:7]	L	√	L
DV[16:23]	L	L	L
CKX2	√	√	√
CK	√	√	L
DVALID	H	H	H
FIELD	√	√	H
HVALID	√	√	H
VVALID	√	√	H
HS	√	√	H
VS	√	√	H

Note : Data/signal requirements for SSD1502 to interface with PHILIPS SAA7111 and SAA7113 in different output data formats.

Remark:
DVALID is required to tie high.
Unused signal pins should be tied to known condition.

6.11.2 RGB/YCbCr 24-bit Input Signal with External Sync Signal

The input signal is required 24-bit input RGB/YCbCr signal and 3 timing signal to connect as the following Table 7. The decoder can generate the field signal for frame synchronization by VS signal.

Table 7: Signal requirement for RGB/YCbCr 24-bit input interface connection

Signal name	VESA VGA
DV[0:23]	√
CKX2	L
CK	√
DVALID/DE	√
FIELD	√ (1)
HVALID	H
VVALID	H
HS	√
VS	√

(1) This pin is required for the field stereo mode only.

Remark: HVALID and VVALID are required to tie high.

6.11.3 Serial interface signal

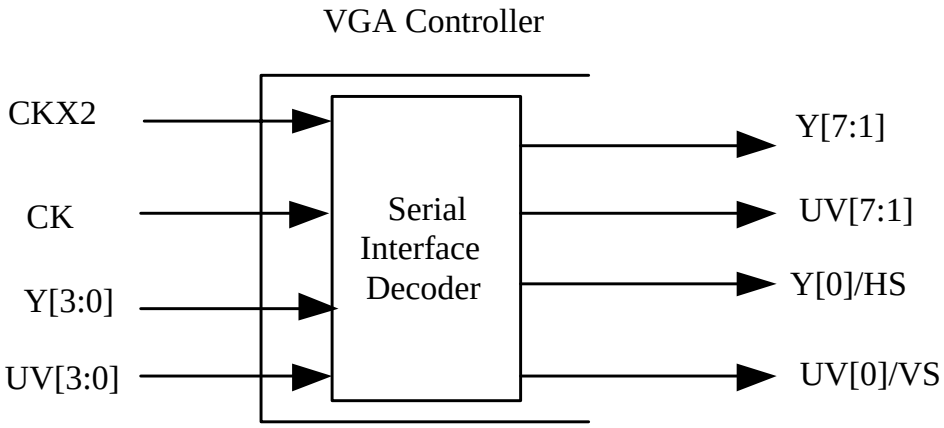


Figure 13: 10-wire serial interface

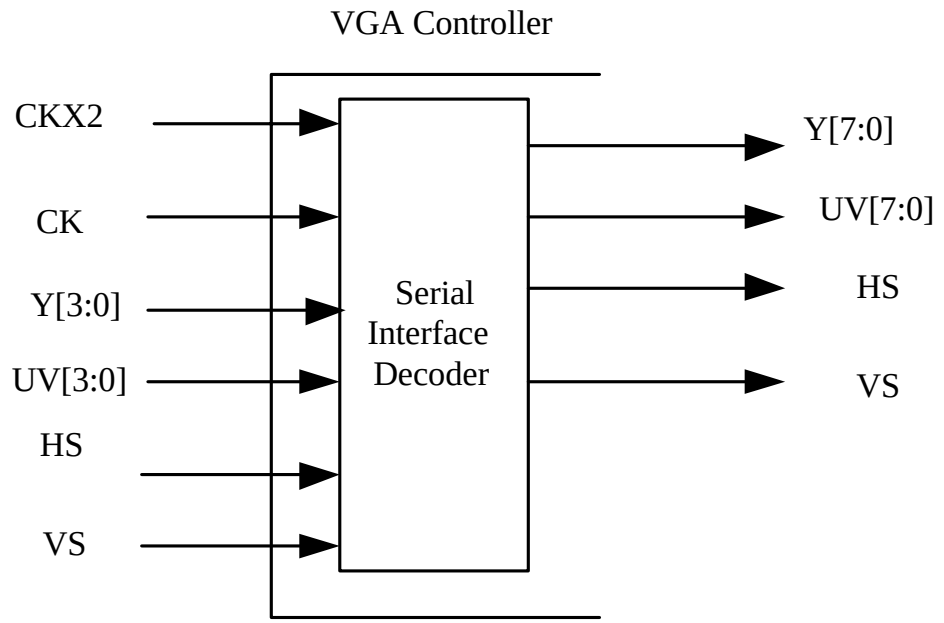


Figure 14: 12-wire serial interface

The different serial interface connections are shown as Figure 13 and Figure 14. This interface format is used for multiplexing the Y and UV component in the higher clock rate. The multiplexed signal will de-multiplex internal into CIRR601 YUV 422 format. For the 6/10-wire serial interface, the HS (VS) signal will be embedded into the LSB of 8-bit Y(UV) component (i.e. Y[0]/UV[0]). It will then be encoded into Y[0:1] (UV[0:1]) signal.

Table 8: Signal requirement for 10/12-wire serial interface format.

Signal name	10-wire	12-wire
Y[0]	√	√
Y[1]	√	√
Y[2]	√	√
Y[3]	√	√
UV[0]	√	√
UV[1]	√	√
UV[2]	√	√
UV[3]	√	√
CLKX2	√	√
CLK	√	√
HS	H	√
VS	H	√

Remark: DVALID, HVALID and VVALID are required to tie high.

6.12 Analog Circuits

6.12.1 D/A Converter

8-bit D/A full scale current can be controlled by external reference resistor R_E. The output maximum voltage V_{OUT} does not exceed 1V. Output current of DAC will be inversed in the line. For example, if one frame is driven with row 0 low, row 1 high, and row 2 low, then the following frame must have row 0 high, row 1 low, and row 2 high. The output inverse can support both dc and ac driving mode. The connection of the output signal and timing output of DAC is shown in the following figures.

Figure 15: DAC Output Connection for the external component

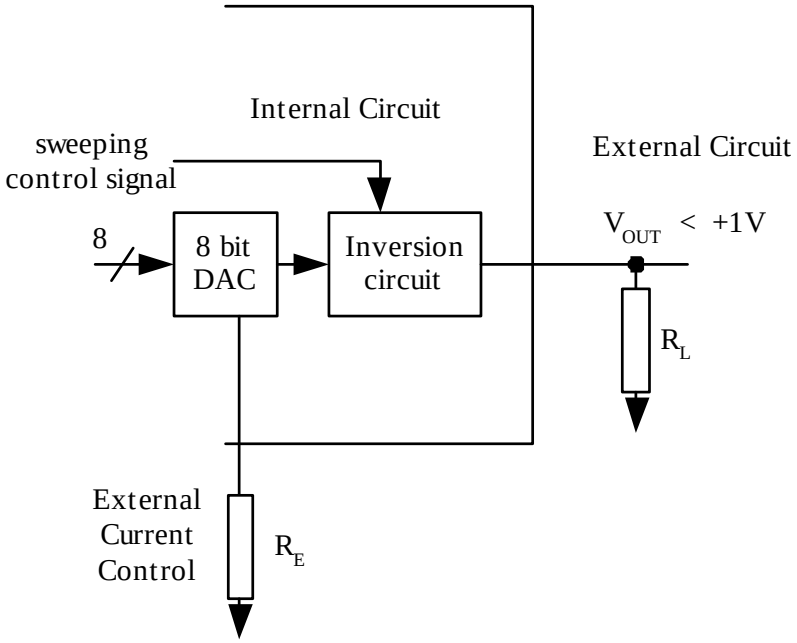


Figure 16: Output Voltage Level versus timing of DAC output in AC driving mode

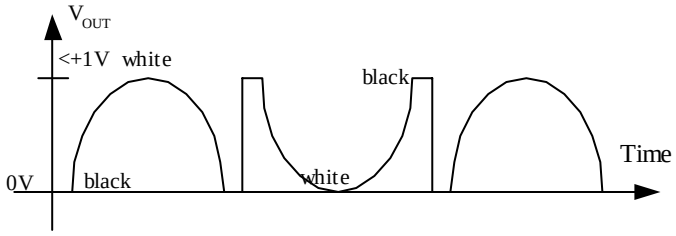
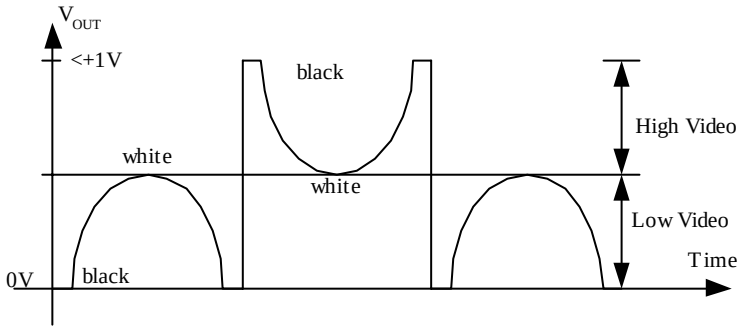


Figure 17: Output Voltage Level versus timing of DAC output in DC driving mode



6.12.2 Power Down Control

D/A can be power down by control register.

6.12.3 External Capacitors

External 0.1uF capacitors are required in COMP1 and REFIO pin.

7 Internal Register Description

Table 9 – Internal Register Table

Address	Function	Note
0X00 ~ 0X3F	Global and TG Control Register	64bytes
0X40 ~ 0X7F	Buffer Control Register	64bytes
0X80 ~ 0XBF	DSP Control Register / DV Display Register	64bytes
0XC0 ~ 0XFF	Digital Video Interface Control Register	64bytes

7.1 Global and TG Control Register

REG[01h]

Bit	7	6	5	4	3	2	1	0
	PWMCLK Force High	PWNCLK Duty Control	0	PWMCLK enable	0	0	0	0
Type	RW	RW	NA	RW	NA	NA	NA	NA
Reset state	0	0	0	1	0	0	0	0

Bit 7: PWMCLK Force High
When this bit = 1, RGB_BK pin output high
When this bit = 0, RGB_BK pin output will be controlled PWM module

Bit 6: PWMCLK DUTY Control
When this bit = 1, PWMCLK duty cycle will controlled by external pin BK_UP and BK_DOWN. BK_UP will increase the high period in RGB_BK output, BK_DOWN versus vice.
When this bit = 0, PWMCLK duty cycle will control by REG[03]

Bit 4: PWMCLK enable
When this bit = 1, PWMCLK is enabled in PWM module
When this bit = 0, PWMCLK is disabled in PWM module

REG[02h]

Bit	7	6	5	4	3	2	1	0
	PWMCLK Source Divide Selection	PWMCLK Source Divide Selection	PWMCLK Source Divide Selection	PWMCLK Source Divide Selection	0	0	0	0
Type	RW	RW	RW	RW	NA	NA	NA	NA
Reset state	0	0	0	0	0	0	0	0

Bit 7-4 : PWMCLK source Divide Selection
This register is used for control the clock source of PWM module.

4’b0000	clk
4’b0001	clk divide by 2
4’b0010	clk divide by 4
4’b0011	clk divide by 8
4’b0100	clk divide by 16
4’b0101	clk divide by 32
4’b0110	clk divide by 64
4’b0111	clk divide by 128
4’b1000	clk divide by 256
4’b1001	clk divide by 512
4’b1010	clk divide by 1024
4’b1011	clk divide by 2048
Otherwise	clk divide by 2048

REG[03h]

Bit	7	6	5	4	3	2	1	0
	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection	PWM clock duty cycle selection
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	0	0	0	0	0	0	0

Bit 7-0: PWM clock duty cycle selection

This register is used for control duty cycle of RBG_BK pin PWM output

8'h00	0 high and 256 low
8'h01	1 high and 255 low
8'h02	2 high and 254 low
.....	.....
8'hFF	255 high and 1 low

REG[04h]

Bit	7	6	5	4	3	2	1	0
	VCOM sweep position Bit 7	VCOM sweep position Bit 6	VCOM sweep position Bit 5	VCOM sweep position Bit 4	VCOM sweep position Bit 3	VCOM sweep position Bit 2	VCOM sweep position Bit 1	VCOM sweep position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

REG[05h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	VCOM sweep position Bit 9	VCOM sweep position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: VCOM sweep position

This register is used for control the VCOM signal sweep position. It is only work when REG[1F] bit 4 = 0.

REG[06h]

Bit	7	6	5	4	3	2	1	0
	Data Fetch Position Bit 7	Data Fetch Position Bit 6	Data Fetch Position Bit 5	Data Fetch Position Bit 4	Data Fetch Position Bit 3	Data Fetch Position Bit 2	Data Fetch Position Bit 1	Data Fetch Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	1	0	1	1	0

REG[07h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Data Fetch Position Bit 9	Data Fetch Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: Data Fetch Position

This register is used to control data fetch timing from the memory line buffer. This register setting will affect the data output position to the display panel.

REG[08h]

Bit	7	6	5	4	3	2	1	0
	VST Rising Edge Position Bit 7	VST Rising Edge Position Bit 6	VST Rising Edge Position Bit 5	VST Rising Edge Position Bit 4	VST Rising Edge Position Bit 3	VST Rising Edge Position Bit 2	VST Rising Edge Position Bit 1	VST Rising Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	1	0	0	1	0

REG[09h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	VST Rising Edge Position Bit 9	VST Rising Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: VST Rising Edge Position

This register is for setting VST rising edge position.

REG[0Ah]

Bit	7	6	5	4	3	2	1	0
	VST Falling Edge Position Bit 7	VST Falling Edge Position Bit 6	VST Falling Edge Position Bit 5	VST Falling Edge Position Bit 4	VST Falling Edge Position Bit 3	VST Falling Edge Position Bit 2	VST Falling Edge Position Bit 1	VST Falling Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	1	0	0	0	1	1	0

REG[0Bh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	VST Falling Edge Position Bit 9	VST Falling Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: VST Falling Edge Position
This register is for setting VST falling edge position.

REG[0Ch]

Bit	7	6	5	4	3	2	1	0
	VCK Rising Edge Position Bit 7	VCK Rising Edge Position Bit 6	VCK Rising Edge Position Bit 5	VCK Rising Edge Position Bit 4	VCK Rising Edge Position Bit 3	VCK Rising Edge Position Bit 2	VCK Rising Edge Position Bit 1	VCK Rising Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	0	0	0	0	0

REG[0Dh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	VCK Rising Edge Position Bit 9	VCK Rising Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: VCK Rising Edge Position
This register is for setting VCK rising edge position.

REG[0Eh]

Bit	7	6	5	4	3	2	1	0
	VCK Falling Edge Position Bit 7	VCK Falling Edge Position Bit 6	VCK Falling Edge Position Bit 5	VCK Falling Edge Position Bit 4	VCK Falling Edge Position Bit 3	VCK Falling Edge Position Bit 2	VCK Falling Edge Position Bit 1	VCK Falling Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	0	0	1	0	0

REG[0Fh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	VCK Falling Edge Position Bit 9	VCK Falling Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: VCK Falling Edge Position
This register is for setting VCK falling edge position.

REG[10h]

Bit	7	6	5	4	3	2	1	0
	HST Rising Edge Position Bit 7	HST Rising Edge Position Bit 6	HST Rising Edge Position Bit 5	HST Rising Edge Position Bit 4	HST Rising Edge Position Bit 3	HST Rising Edge Position Bit 2	HST Rising Edge Position Bit 1	HST Rising Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	1	0	1	0	1

REG[11h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	HST Rising Edge Position Bit 9	HST Rising Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: HST Rising Edge Position
This register is for setting HST rising edge position.

REG[12h]

Bit	7	6	5	4	3	2	1	0
	HST Falling Edge Position Bit 7	HST Falling Edge Position Bit 6	HST Falling Edge Position Bit 5	HST Falling Edge Position Bit 4	HST Falling Edge Position Bit 3	HST Falling Edge Position Bit 2	HST Falling Edge Position Bit 1	HST Falling Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	1	0	1	1	1

REG[13h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	HST Falling Edge Position Bit 9	HST Falling Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: HST Falling Edge Position
This register is for setting HST falling edge position.

REG[14h]

Bit	7	6	5	4	3	2	1	0
	EN Rising Edge Position Bit 7	EN Rising Edge Position Bit 6	EN Rising Edge Position Bit 5	EN Rising Edge Position Bit 4	EN Rising Edge Position Bit 3	EN Rising Edge Position Bit 2	EN Rising Edge Position Bit 1	EN Rising Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	0	1	1	0	0

REG[15h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	EN Rising Edge Position Bit 9	EN Rising Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: EN Rising Edge Position
This register is for setting EN rising edge position.

REG[16h]

Bit	7	6	5	4	3	2	1	0
	EN Falling Edge Position Bit 7	EN Falling Edge Position Bit 6	EN Falling Edge Position Bit 5	EN Falling Edge Position Bit 4	EN Falling Edge Position Bit 3	EN Falling Edge Position Bit 2	EN Falling Edge Position Bit 1	EN Falling Edge Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	1	1	0	0	0	0

REG[17h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	EN Falling Edge Position Bit 9	EN Falling Edge Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	1	0

Bits 9-0: EN Falling Edge Position

This register is for setting EN falling edge position.

REG[18h]

Bit	7	6	5	4	3	2	1	0
	Second New Line Start Position Bit 7	Second New Line Start Position Bit 6	Second New Line Start Position Bit 5	Second New Line Start Position Bit 4	Second New Line Start Position Bit 3	Second New Line Start Position Bit 2	Second New Line Start Position Bit 1	Second New Line Start Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	1	0	1	0	0	0	0

REG[19h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Second New Line Start Position Bit 9	Second New Line Start Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	1	1

Bits 9-0: New Second Line Start Position

This register is only used for the generation of the new second new line start position to the panel in the interlace video source. This position helps for generating the output timing control signals.

REG[1Ah]

Bit	7	6	5	4	3	2	1	0
	New Frame Position Bit 7	New Frame Position Bit 6	New Frame Position Bit 5	New Frame Position Bit 4	New Frame Position Bit 3	New Frame Position Bit 2	New Frame Position Bit 1	New Frame Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	1	0

REG[1Bh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	New Frame Position Bit 9	New Frame Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: New Frame Position

This register is for setting the new frame position after Vsync signal which go to a non valid data interval. This register only function when REG[C0] bit 7 = 1.

REG[1Ch]

Bit	7	6	5	4	3	2	1	0
	0	SLEEP Control	RGT Control	DWN Control	Power Down Control	Disable VCOM Frame Change	VCOM Polarity	Disable Internal VCOM
Type	NA	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	1	0	0	0	0

Bit 6: SLEEP Control
This bit is for display panel control.
When this bit = 1, SLEEP pin will drive high.
When this bit = 0, SLEEP pin will drive low.

Bit 5: RGT Control
This bit is for display panel control.
When this bit = 1, RGT pin will drive high.
When this bit = 0, RGT pin will drive low.

Bit 4: DWN Control
This bit is for display panel control.
When this bit = 1, DWN pin will drive high.
When this bit = 0, DWN pin will drive low.

Bit 3: Power Down Control
When this bit = 1, power down will be activated.
When this bit = 0, normal.

Bit 2: Disable VCOM Frame Change
When this bit = 1, VCOM does not sweep after in each new frame.
When this bit = 0, VCOM sweeps after in each new frame. (Normal mode)

Bit 1: VCOM polarity
This bit is for controlling video signal sweeping vs VCOM polarity.
When this bit = 1, internal VCOM high for sweeping output video signal.
When this bit = 0, internal VCOM low for sweeping output video signal.

Bit 0: Disable internal VCOM change
When this bit = 1, internal VCOM does not sweep at each new line
When this bit = 0, internal VCOM sweeps when line change. (Normal mode)

REG[1Dh]

Bit	7	6	5	4	3	2	1	0
	0	INV CLKX2	SKEW Control CLKX2	SKEW Control CLKX2	SRC CLK	INV CLK	SKEW Control CLK	SKEW Control CLK
Type	NA	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bit 6: INV CLKX2
This bit is for controlling the inversion of CLKX2
When this bit = 1, the inversion of CLKX2 is enabled.
When this bit = 0, Normal.

Bits 5-4: SKEW Control CLKX2
This bit is for phase adjustment
2'b00: No phase delay
2'b01-2'b11: Approximately 2ns per step

Bit 3: SRC CLK
This bit is for CLK source selection
When this bit = 1, source of CLK is generated by CLKX2 signal.
When this bit = 0, source of CLK is external input pin CLK.

Bit 2: INV CLK
This bit is for controlling the inversion of CLK
When this bit = 1, the inversion of CLK is enabled.
When this bit = 0, Normal.

Bits 1-0: SKEW Control CLK
This bit is for phase adjustment
2'b00: No phase delay
2'b01-2'b11: Approximately 2ns per step

REG[1Eh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	HCLK Control	Disable Gate HCLK	INV CLK	SKEW Control HCLK	SKEW Control HCLK
Type	NA	NA	NA	RW	RW	RW	RW	RW
Reset state	0	0	0	1	1	0	0	0

Bit 4: HCLK Control
This bit is for controlling sync of HCLK in each line.
When this bit = 1, without synchronization.
When this bit = 0, normal.

Bit 3: Disable Gate HCLK
This bit is for gating of the HCLK signal when EN is low.
When this bit = 1, disable the gating of HCLK.
When this bit = 0, normal.

Bit 2: INV HCLK
This bit is for controlling the inversion of HCLK
When this bit = 1, the inversion of HCLK is enabled.
When this bit = 0, normal.

Bits 1-0: SKEW Control HCLK
This bit is for phase adjustment
2'b00: No phase delay
2'b01-2'b11: Approximately 2ns per step

REG[1Fh]

Bit	7	6	5	4	3	2	1	0
	DAC PWDA	DAC PWDD	DAC REFIO	DAC Mode Control	DAC DC tuning	DAC DC tuning	DAC DC tuning	DAC DC tuning
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	1	0	0	0	0	0

Bit 7: DAC PWDA
This bit is for controlling power down analog part of DAC
When this bit = 1, power down the analog part of DAC.
When this bit = 0, normal.

Bit 6: DAC PWDD
This bit is for controlling power down digital part of DAC
When this bit = 1, power down the digital part of DAC.
When this bit = 0, normal.

Bit 5: Bandgap Voltage Control
This bit is for controlling source of voltage reference
When this bit = 1, select the internal bandgap voltage reference.
When this bit = 0, select the external voltage reference by REFIO pin.

Bit 4: DAC Mode Control
This bit is for controlling VCOM driving mode.
When this bit = 1, VCOM DC driving mode will be activated.
When this bit = 0, VCOM AC driving mode will be activated.

Bits 3-0: DAC DC tuning
These bits are for controlling DAC offset level in the VCOM DC mode.

REG[20h]

Bit	7	6	5	4	3	2	1	0
	0	0	Test Probe0 Control	Test Probe0 Control	Test Probe0 Control	Test Probe0 Control	Test Probe0 Control	Test Probe0 Control
Type	NA	NA	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 5-0: Test Probe0 Control
This register is for internal test only.

REG[21h]

Bit	7	6	5	4	3	2	1	0
	0	0	Test Probe1 Control	Test Probe1 Control	Test Probe1 Control	Test Probe1 Control	Test Probe1 Control	Test Probe1 Control
Type	NA	NA	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 5-0: Test Probe1 Control
This register is for internal test only.

7.2 Buffer Control Register

REG[40h]

Bit	7	6	5	4	3	2	1	0
	TestPN enable	TestPN MUX Control	TestPN MUX Control	TestPN MUX Control	0	TestPN Frontend	Color Mode	Color Mode
Type	RW	RW	RW	RW	NA	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bit 7: TestPN enable
This register is for controlling the internal test pattern generation.
When this bit = 1, embedded test pattern will be generated.
When this bit = 0, normal

Bits 6-4: TestPN MUX Control
This register is the option control for different type of test pattern.

Bit 2: TestPN Frontend
This register is for internal test only. It **MUST be** kept at 0 in normal operation.

Bits 1-0: Color Mode
This register is for selection of embedded test pattern when TestPN enable is equal to 1.

Option	Pattern Type
00	Color bar
01	Checkbox
10	Gradient Up
11	Crosshatch

REG[41h]

Bit	7	6	5	4	3	2	1	0
	0	0	Stereo Mode Control	Stereo Mode Control	Median Filter Control	VCOM Flip Control	Deinterlace Enable	Internal Test
Type	NA	NA	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 5-4: Stereo Mode Control
This register is for controlling different Video Stereo Modes.

Option	Type
00, 01	Normal Operation
10	Field Video Stereo
11	Line Video Stereo

Bit 3: Median Filter Control
This bit is for selection of different deinterlace mode.
When this bit = 1, median filter option is selected for deinterlacing.
When this bit = 0, line double option is selected for deinterlacing.

Bit 2: VCOM Flip Control
This bit is for controlling VCOM Flipping versus new frame signal. It is mainly used for Field Stereo mode to provide an appropriate VCOM flipping to display panel.
When this bit = 1, VCOM will flip per two new frame signal pulse.
When this bit = 0, VCOM will flip per each new frame signal pulse.

Bit 1: Deinterlace Enable
This bit is for controlling the deinterlace option
When this bit = 1, deinterlace is activated.
When this bit = 0, deinterlace is deactivated.

Bit 0: Internal Test
This register is for internal test only. It **MUST** keep 0 in normal operation.

7.3 DV Display Register

REG[70h]

Bit	7	6	5	4	3	2	1	0
	Horizontal Crop Start Position Bit 7	Horizontal Crop Start Position Bit 6	Horizontal Crop Start Position Bit 5	Horizontal Crop Start Position Bit 4	Horizontal Crop Start Position Bit 3	Horizontal Crop Start Position Bit 2	Horizontal Crop Start Position Bit 1	Horizontal Crop Start Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

REG[71h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Horizontal Crop Start Position Bit 9	Horizontal Crop Start Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: Horizontal Crop Start Position
The register is for controlling Horizontal Crop Start Position

REG[72h]

Bit	7	6	5	4	3	2	1	0
	Horizontal Crop End Position Bit 7	Horizontal Crop End Position Bit 6	Horizontal Crop End Position Bit 5	Horizontal Crop End Position Bit 4	Horizontal Crop End Position Bit 3	Horizontal Crop End Position Bit 2	Horizontal Crop End Position Bit 1	Horizontal Crop End Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	1	1	1	1	1	1	1

REG[73h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Horizontal Crop End Position Bit 9	Horizontal Crop End Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	1	0

Bits 9-0: Horizontal Crop End Position
The register is for controlling Horizontal Crop End Position

REG[74h]

Bit	7	6	5	4	3	2	1	0
	Vertical Crop Start Position Bit 7	Vertical Crop Start Position Bit 6	Vertical Crop Start Position Bit 5	Vertical Crop Start Position Bit 4	Vertical Crop Start Position Bit 3	Vertical Crop Start Position Bit 2	Vertical Crop Start Position Bit 1	Vertical Crop Start Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

REG[75h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Vertical Crop Start Position Bit 9	Vertical Crop Start Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 9-0: Vertical Crop Start Position
The register is for controlling Vertical Crop Start Position

REG[76h]

Bit	7	6	5	4	3	2	1	0
	Vertical Crop End Position Bit 7	Vertical Crop End Position Bit 6	Vertical Crop End Position Bit 5	Vertical Crop End Position Bit 4	Vertical Crop End Position Bit 3	Vertical Crop End Position Bit 2	Vertical Crop End Position Bit 1	Vertical Crop End Position Bit 0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	0	1	1	1	1	1

REG[77h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Vertical Crop End Position Bit 9	Vertical Crop End Position Bit 8
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	1

Bits 9-0: Vertical Crop End Position
The register is for controlling Vertical Crop End Position

REG[78h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	Field Ajustment EVEN	Field Adjustment ODD
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bit 1: Odd Field Adjustment
This bit is for controlling 1 line delay capture in odd field
When this bit = 1, vertical crop start and end position will shift one in odd field only.
When this bit = 0, normal operation.

Bit 0: Even Field Adjustment
This bit is for controlling 1 line delay capture in even fields
When this bit = 1, vertical crop start and end position will shift one in the even field only.
When this bit = 0, normal operation.

Remark: The 1 delay capture is required in different field when the interlace video signal without HVALID and VVALID control signal. It is because interlace mode HS and VS have a half line shift to indicate the field change.

7.4 DSP Control Register

REG[81h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	Gamma Enable
Type	NA	NA	NA	NA	NA	NA	NA	RW
Reset state	0	0	0	0	0	0	0	0

Bit 1: Gamma Enable
This bit is to enable the Gamma Correction.
When this bit = 1, Gamma Correction is enabled.
When this bit = 0, Gamma Correction is disabled.

REG[82h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color	Gamma Look-up Table LUT0/ Low Value of Color
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 7-0: Gamma Look-up Table LUT0.
This register is used for the Gamma Look-up Table LUT0 and low bound of the color input.

REG[83h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1	Gamma Look-up Table LUT1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	1	0	1	1	0	1	1

Bits 7-0: Gamma Look-up Table LUT1.
This register is used for Gamma Look-up Table LUT1.

REG[84h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2	Gamma Look-up Table LUT2
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	0	0	0	0	0	0	0

Bits 7-0: Gamma Look-up Table LUT2.
This register used for Gamma Look-up Table LUT2.

REG[85h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3	Gamma Look-up Table LUT3
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	0	0	1	1	1	0	1

Bits 7-0: Gamma Look-up Table LUT3.
This register used for Gamma Look-up Table LUT3.

REG[86h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4	Gamma Look-up Table LUT4
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	0	1	1	0	1	0	1

Bits 7-0: Gamma Look-up Table LUT4.
This register used for Gamma Look-up Table LUT4.

REG[87h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5	Gamma Look-up Table LUT5
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	0	0	1	0	1	0

Bits 7-0: Gamma Look-up Table LUT5.
This register used for Gamma Look-up Table LUT5.

REG[88h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6	Gamma Look-up Table LUT6
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	0	1	1	1	1	0

Bits 7-0: Gamma Look-up Table LUT6.
This register used for Gamma Look-up Table LUT6.

REG[89h]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7	Gamma Look-up Table LUT7
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	1	0	1	1	1	1

Bits 7-0: Gamma Look-up Table LUT7.
This register used for Gamma Look-up Table LUT7.

REG[8Ah]

Bit	7	6	5	4	3	2	1	0
	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color	Gamma Look-up Table LUT8/ High Value of Color
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	1	1	1	1	1	1	1	1

Bits 7-0: Gamma Look-up Table LUT8.
This register used for Gamma Look-up Table LUT8 and upper bound of the color input.

REG[90h]

Bit	7	6	5	4	3	2	1	0
	CSC Mode	CSC Mode	RGB to YCBCR Enable	YCBCR to RGB Enable	Monochrome	Vertical Scale	Horizontal Scale	Horizontal Scale
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 7-6: CSC Mode

This register is for the selection of color space conversion

Option	Color Space Conversion
00	SMTPE 170M
01	CIRR 601
10	BT 601
11	Not allowed

Bit 5: RGB to YCBCR Enable

This bit is enable the RGB to YCBCR color space conversion

When this bit = 1, RGB to YCBCR color space conversion is enabled.

When this bit = 0, normal.

Bit 4: YCBCR to RGB Enable

This bit enables the YCBCR to RGB color space conversion

When this bit = 1, YCBCR to RGB color space conversion is enabled.

When this bit = 0, normal.

Bit 3: Monochrome

This bit is for setting monochrome color output. In RGB video signal, REG[90] bit 5 MUST be set at 1.

When this bit = 1, monochrome filter is enabled.

When this bit = 0, normal.

Bit 2: Vertical Scale

The register is for selection of the Vertical scale.

Vertical crop start REG[75-74] and vertical crop end register setting REG[77-76] must be set appropriately for the selected vertical scale..

Cropped Vertical Size = REG[77-76] – REG[75-74] + 1;

Option	Cropped Vertical Size	Vertical Scale
Interlace Video Source		
0	240	1:1
1	288	6:5
Progressive Video Source		
0	240	1:1
1	576	6:5

Bits 1-0: Horizontal Scale

The register is for selection of Horizontal scale.

Horizontal crop start REG[71-70] and horizontal crop end register setting REG[73-72].must be set appropriately for the selected horizontal scale.

Cropped Horizontal Size = REG[73-72] – REG[71-70] + 1;

Option	Cropped Horizontal Size	Horizontal Scale
00	640	1:1
01	768	6:5
10	720	9:8
11	704	11:10

REG[98h]

Bit	7	6	5	4	3	2	1	0
	Y Component Offset	Y Component Offset	Y Component Offset	Y Component Offset	Y Component Offset	Y Component Offset	Y Component Offset	Y Component Offset
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 7-0: Y component offset
This register is for tuning the offset in the Y component. It is only work when YCBCR to RGB color space conversion is enabled.

REG[99h]

Bit	7	6	5	4	3	2	1	0
	CB Component Offset	CB Component Offset	CB Component Offset	CB Component Offset	CB Component Offset	CB Component Offset	CB Component Offset	CB Component Offset
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 7-0: CB component offset
This register is for tuning the offset in the Y component. It is only work when YCBCR to RGB color space conversion is enabled.

REG[9Ah]

Bit	7	6	5	4	3	2	1	0
	CR Component Offset	CR Component Offset	CR Component Offset	CR Component Offset	CR Component Offset	CR Component Offset	CR Component Offset	CR Component Offset
Type	RW	RW	RW	RW	RW	RW	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bits 7-0: CR component offset
This register is for tuning the offset in the Y component. It is only work when YCBCR to RGB color space conversion is enabled.

REG[9Bh]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0
Type	NA	NA	NA	NA	NA	NA	NA	NA
Reset state	0	0	0	0	0	0	0	0

REG[9Ch]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0
Type	NA	NA	NA	NA	NA	NA	NA	NA
Reset state	0	0	0	0	0	0	0	0

7.5 Digital Video Interface Control Register

REG[C0h]

Bit	7	6	5	4	3	2	1	0
	Select Frame Pulse Generation	Internal Line & Frame Generation	0	Field Signal Generation	Field Signal Control	Input Data Width Selection	Input Data Width Selection	0
Type	RW	RW	NA	RW	RW	RW	RW	NA
Reset state	0	0	0	1	0	1	0	0

Bit 7: Select Frame Pulse Generation
This bit is for controlling the internal frame pulse generation
When this bit = 1, the frame pulse signal is generated by internal Vsync Signal.
When this bit = 0, the frame pulse signal is generated by Field Signal.

Bit 6: Internal Line and Frame Signal Generation
This bit is for internal testing only. In normal operation, it **MUST** be set to 0.

Bit 4: Field Signal Generation
This bit is for selection of Field signal generation when REG[C1] bit 3 = 0 and REG[C2] bit 6 = 0.

When this bit = 1, the Field signal is generated by the internal new frame signal.
When the progressive video source is operating in the source field stereo mode without an external FIELD signal control, this bit **MUST** be set at 0.
When this bit = 0, the Field signal is selected by external FIELD input pin.

Bit 3: Field Signal Control
This bit is for control the polarity of FIELD signal.
When this bit = 1, inverse the input FIELD signal.
When this bit = 0, bypass the input FIELD signal.

Bits 2-1: Input Data Width Selection
This register is for setting input data width

Option	Input Data Width
00	8-bit
01	16-bit
10, 11	24-bit

REG[C1h]

Bit	7	6	5	4	3	2	1	0
	0	0	Active Signal Control	Active Signal Control	Active Signal Control	SAV/ EAV Field Control	0	Active Video Region Control
Type	NA	NA	RW	RW	RW	RW	NA	RW
Reset state	0	0	0	0	0	0	0	1

Bit 5-3: Active Signal Control
This register is for the selection of the active signal.

Option	Active Signal
xx1	Decoded from SAV/EAV packet
x10	Control by HVALID only
000	Control by HVALID and DVALID/VVALID which depends on REG[C1] bit 1.
100	VVALID will not be used as control signal

Bit 2: SAV-EAV Field Control
This bit is for the selection of the Field signal
When this bit = 1, the Field signal is generated by the SAV-EAV packet

When this bit = 0, the generation of the Field signal depends on the REG[C0] bit 4 and REG[C1] bit 6.

Bit 0: Active Video Region Control
This bit is for controlling the active video region into video data processing.
When this bit = 1, the active video is control by the HVALID and DVALID signal.
When this bit = 0, the active video is control by the HVALID and VVALID signal.

REG[C2h]

Bit	7	6	5	4	3	2	1	0
	0	Field SYNC Control	0	VSYNC Signal Control	HSYNC Signal Control	VSYNC Polarity Control	HSYNC polarity Control	0
Type	NA	RW	NA	RW	RW	RW	RW	NA
Reset state	0	0	0	0	0	1	0	0

Bit 6: Field SYNC Control
When this bit = 1 and REG[C1] bit 2 = 0, the Field signal is generated by VSYNC and HSYNC.
When this bit = 0, the generation of the Field signal depends on the REG[C0] bit 4.

Bit 4: VSYNC Signal Control
This bit is for controlling the generation of the VSYNC signal
When this bit = 1 and REG[C3] bit 0 = 0, VSYNC is generated by VVALID.
When this bit = 0 and REG[C3] bit 0 = 0, VSYNC is generated by external VS.

Bit 3: HSYNC Signal Control
This bit is for controlling the generation of the HSYNC signal
When this bit = 1 and REG[C3] bit 0 = 0, the HSYNC is generated by HVALID.
When this bit = 0 and REG[C3] bit 0 = 0, the HSYNC is generated by external HS.

Bit 2: VSYNC Polarity Control
This bit is for controlling the polarity of the VSYNC signal
When this bit = 1, inverse the VSYNC signal.
When this bit = 0, bypass the VSYNC signal.

Bit 1: HSYNC Polarity Control
This bit is for controlling the polarity of the HSYNC signal
When this bit = 1, inverse the HSYNC signal.
When this bit = 0, bypass the HSYNC signal.

REG[C3h]

Bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	RGB565 Format Selection	SAV/ EAV SYNC Control
Type	NA	NA	NA	NA	NA	NA	RW	RW
Reset state	0	0	0	0	0	0	0	0

Bit 1: RGB565 format Selection
This bit is for the selection of the RGB565 video input format
When this bit = 1 and REG[C0] bits 2-1 = 0x01, RGB565 video input format is selected.
When this bit = 0, otherwise.

Bit 0: SAV/EAV SYNC control
This bit is for the selection of HSYNC /VSYNC signal
When this bit = 1, HSYNC/VSYNC is generated by the SAV/EAV packet
When this bit = 0, HSYNC/VSYNC depends on REG[C2] bit 4 and bit 3.

8 Maximum Ratings

Table 10: Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Digital Supply Voltage relative to VSS	-0.3 to 3.6	V
AV_{DD}	Analog Supply Voltage relative to VSS	-0.3 to 3.6	V
V_{IN}	Voltage on any pin relative to VSS	-0.3 to VDD+0.3	V
T_{OPT}	Operating Temperature	-30 to +85	^{0}C
T_{STG}	Storage Temperature	-40 to 125	^{0}C

9 DC Characteristics

9.1 Recommended DC Operating Conditions

Table 11: DC Characteristics T_A = 25°C, VDD = 3.3V±5%, VSS=0V

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	Digital Supply Voltage	VDD=AVDD	3.0	3.3	3.6	V
AV_{DD}	Analog Supply Voltage					
V_{IL}	Input low voltage		-	-	$0.3V_{DD}$	V
V_{IH}	Input high voltage		$0.7V_{DD}$	-	-	V
V_{OL}	Output low voltage	4mA buffer, I_{OL}=4mA, 8mA buffer, I_{OL}=8mA (HCK0, HCK1)	-	-	0.4	V
V_{OH}	Output high voltage	4mA buffer, I_{OL}=4mA 8mA buffer, I_{OL}=8mA (HCK0,HCK1)	2.4	-		V
I_{DVDD_slp}	Digital Power supply shutdown current		-20	-	20	uA
I_{AVDD_slp}	Analog Power supply shutdown current		-20	-	20	uA
I_{DVDD}	Digital Power supply operating current	For CLX2 frequency =27MHz	-	5	15	mA
I_{AVDD}	Analog Power supply operating current		-	25	35	mA
IOUT	DAC output current	FDASJ connect to gnd with 3k resistor AC COM mode	5.9	7	8.1	mA

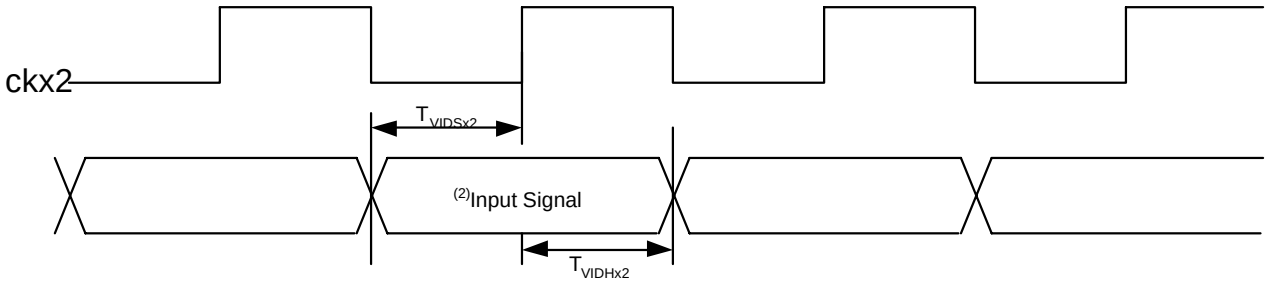
10 AC Characteristics

Table 12: AC Characteristics (Unless otherwise specified, Voltage Referenced to VSS, VDD = 3.3V, TA = -30 to 85°C)

Parameter	Symbol	MIN	TYP	MAX	Units
CKX2 Input Frequency	f_{CKX2}	-	-	36/60[1]	MHz
CKX2 Input Period	t_{CKX2T}	27.8/16.67[1]	-	-	ns
CKX2 and Video Input Data Setup Time	t_{VIDSX2}	5	-	-	ns
CKX2 and Video Input Data Hold Time	t_{VIDHX2}	5	-	-	ns
CK and Video Input Data Setup Time	t_{VIDS}	5	-	-	ns
CK and Video Input Data Hold Time	t_{VIDH}	5	-	-	ns

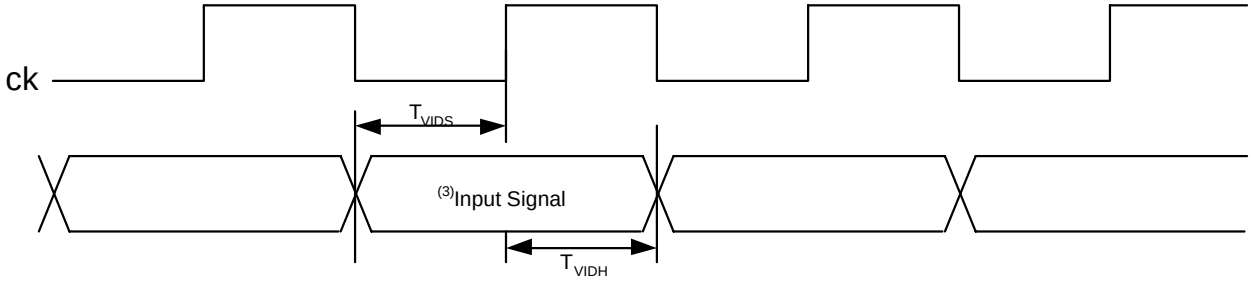
Note (1): This mode is for progressive input video signal source only

Figure 18 -8-bit Video Data Input Timing



Note (2): Input Signal refer to DV[15-8], Dvalid, Hvalid, Vvalid, Vs, Hs, Field

Figure 19 -16/24-bit Video Data Input Timing

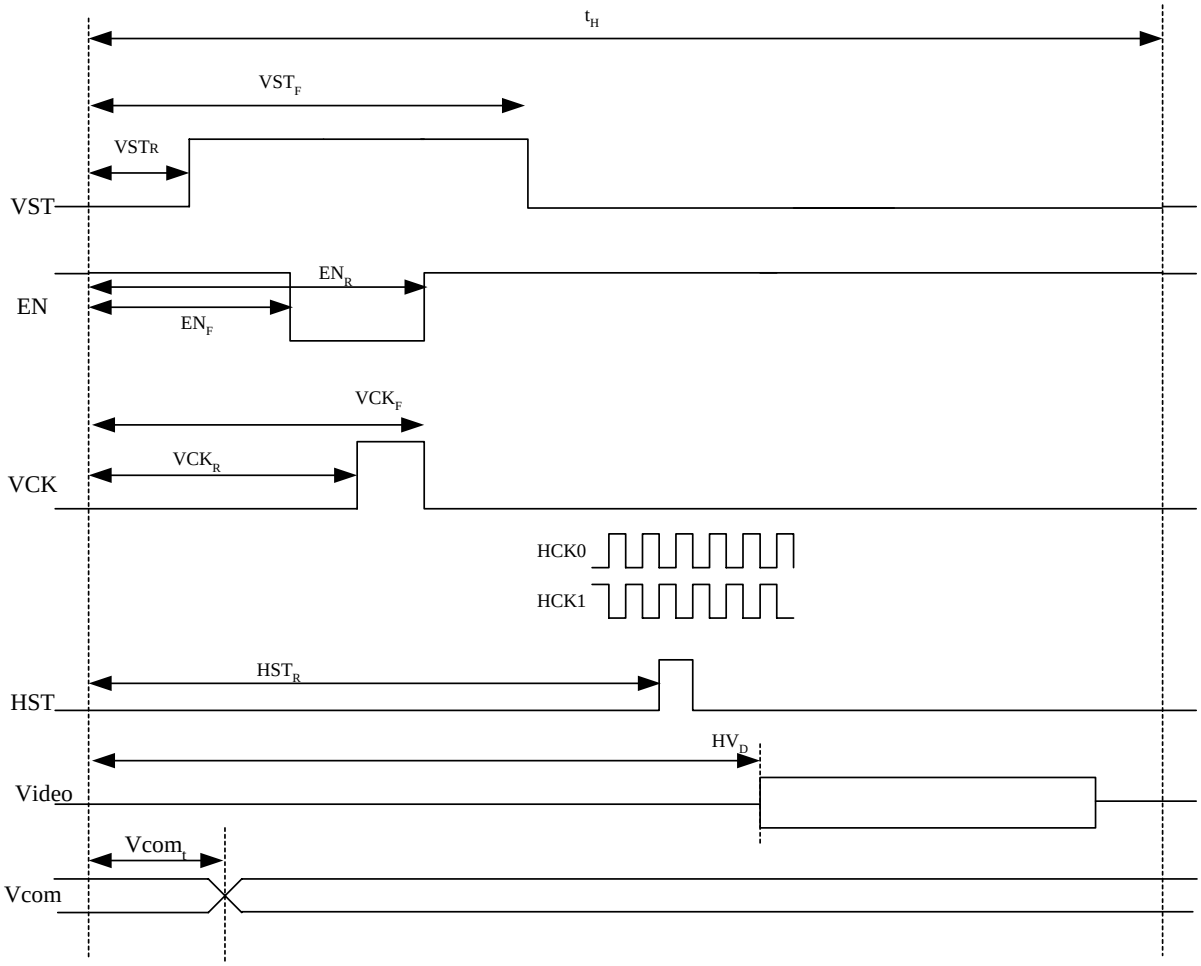


Note (3): Input Signal refer to DV[23-0], Dvalid, Hvalid, Vvalid, Vs, Hs, Field

Table 13: Display Panel Interface Timing

Parameter	Symbol	Min	Typ	Max	Units
Frame Period	t_v		13.3-16.7		ms
Frame rate	$1/t_v$		60-75		Hz
Line Period	t_H		26.7-31.7		µs
Line Frequency	$1/t_H$		31.5-37.5		kHz
Clock Period	t_{CP}		63.5-80		ns
Clock Frequency	$1/t_{CP}$		12.5-15.75		MHz
Video sampling period	t_{PP}	$(t_{CP}/2)-5$		$(t_{CP}/2)+5$	ns
HCK1-HCK2 clock skew	t_{CSK}	-5		5	ns
HST setup	t_{HS}	20			ns
HST hold	t_{HH}	20			ns
VCK high pulse Width	t_{KH}	200			ns
VST setup to VCK	t_{VHS}	100			ns
VST hold after VCK	t_{VHH}	100			ns
VCK to EN delay	t_{KED}	200			ns
EN to VCK delay	t_{EKD}	200			ns
EN to active video delay	t_{EVD}	400			ns
Active video to EN delay	t_{VED}	400			ns

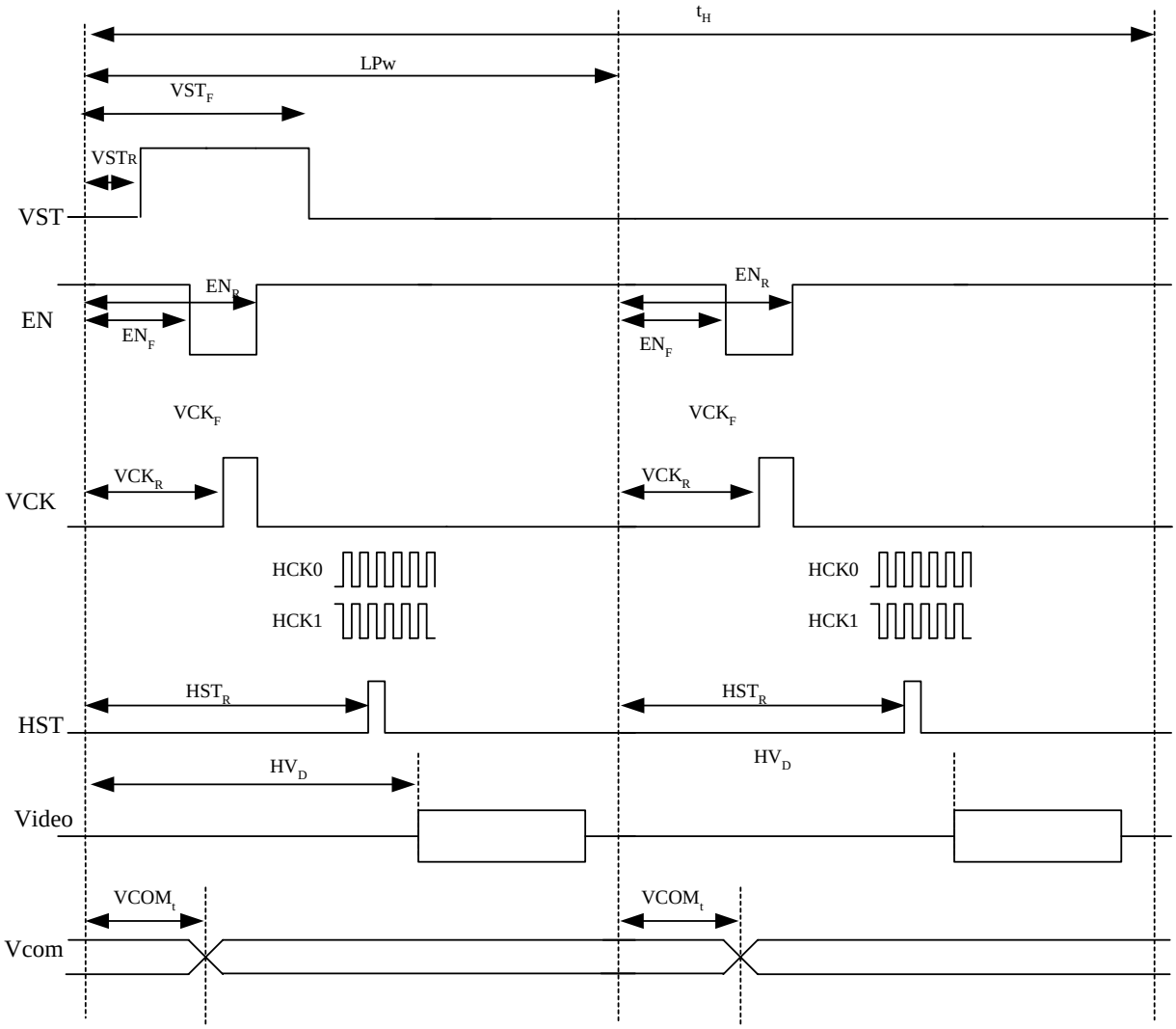
Figure 20: Display Panel Interface Timing Diagram of Progressive Mode



VST_R = VST rising edge (10 bit control register and t_{CP}/2 resolution)
VST_F = VST falling edge (10 bit control register and t_{CP}/2 resolution)
EN_F = VST falling edge (10 bit control register and t_{CP}/2 resolution)
EN_R = VST rising edge (10 bit control register and t_{CP}/2 resolution)
VCK_R = VCK rising edge (10 bit control register and t_{CP}/2 resolution)
VCK_F = VCK falling edge (10 bit control register and t_{CP}/2 resolution)
HST_R = HST rising edge (10 bit control register and t_{CP}/2 resolution)
$VCOM_t$ = VCOM sweeping Transition timing (10 bit control register and t_{CP}/2 resolution)
HV_D = date fetch position (10 bit control register and t_{CP}/2 resolution)

Note: t_{CP} is the period of the HCLK0 and HCLK1 and t_H is the period of the line

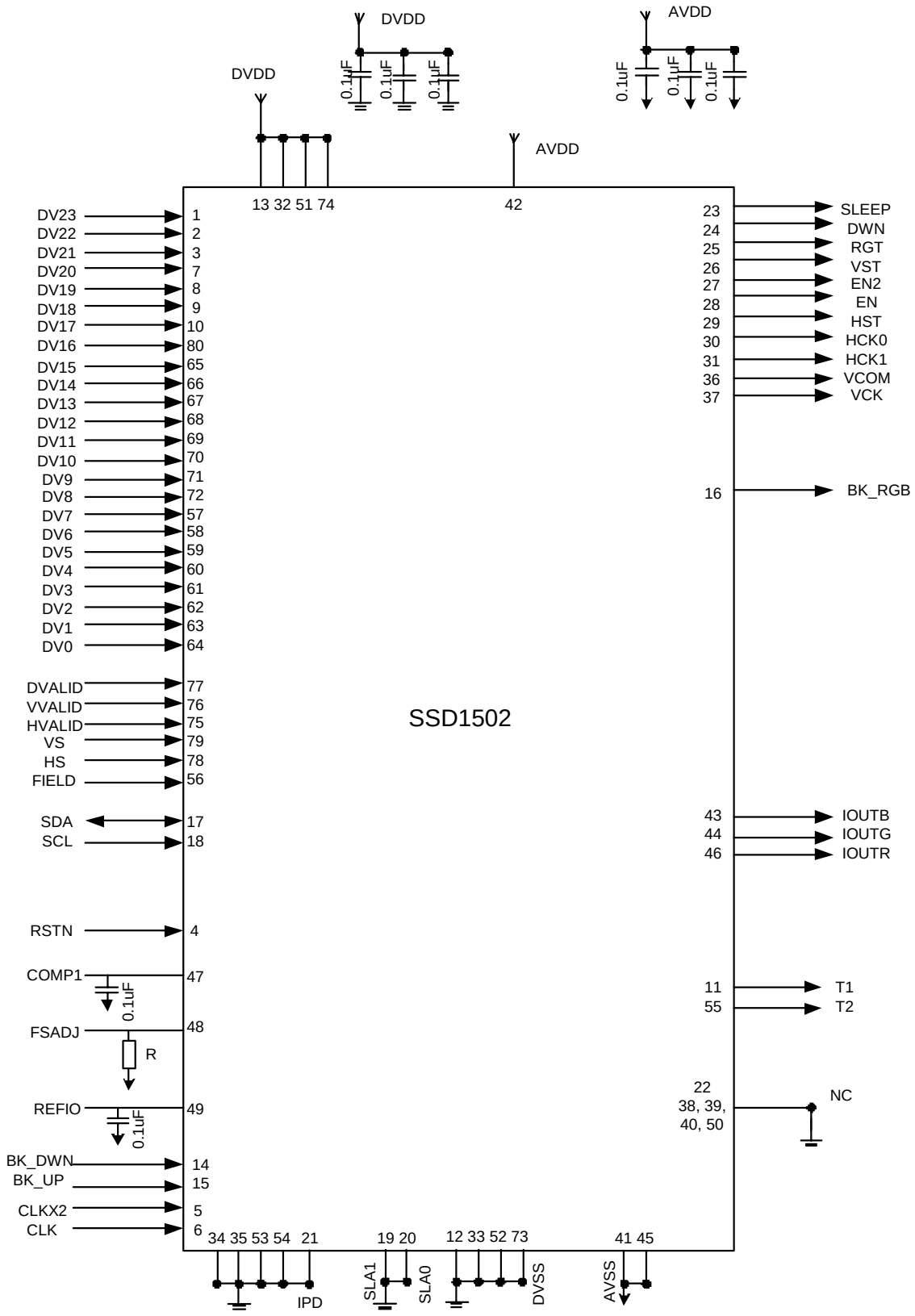
Figure 21 -Display Panel Interface Timing Diagram of Deinterlace Mode



VST_R = VST rising edge (10 bit control register and $t_{CP}/2$ resolution)
VST_F = VST falling edge (10 bit control register and $t_{CP}/2$ resolution)
EN_F = VST falling edge (10 bit control register and $t_{CP}/2$ resolution)
EN_R = VST rising edge (10 bit control register and $t_{CP}/2$ resolution)
VCK_R = VCK rising edge (10 bit control register and $t_{CP}/2$ resolution)
VCK_F = VCK falling edge (10 bit control register and $t_{CP}/2$ resolution)
HST_R = HST rising edge (10 bit control register and $t_{CP}/2$ resolution)
LP_W = Second Line Position (10 bit control register and $t_{CP}/2$ resolution)
$VCOM_t$ = VCOM sweeping Transition timing (10 bit control register and $t_{CP}/2$ resolution)
HV_D = date fetch position (10 bit control register and $t_{CP}/2$ resolution)

Note: t_{CP} is the period of the HCLK0 and HCLK1 and t_H is the period of the line

11 APPLICATION EXAMPLES



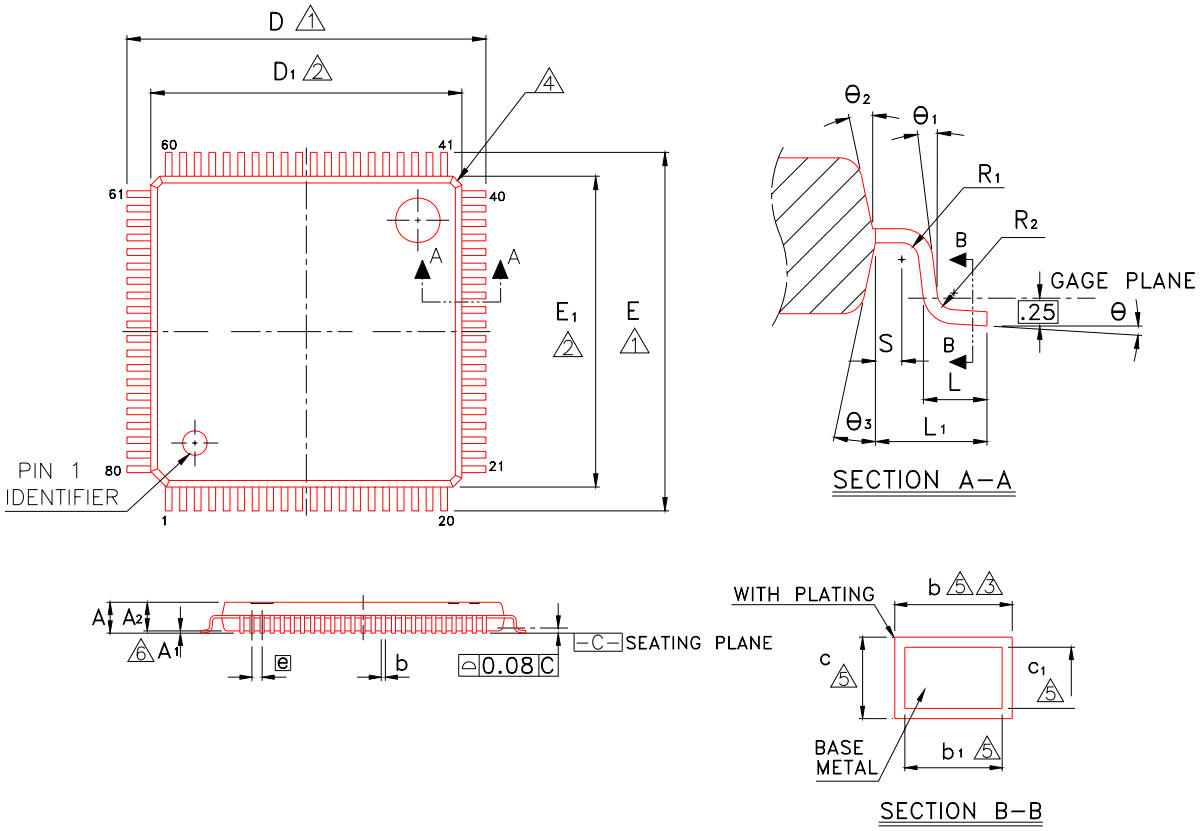
Note.

1. Different input video interface format requires different input connections. Please refer to Section 6.11.

2. For unused input pin DVALID, HVALID, VVALID, VS and HS, they **MUST** tie high. The unused input pin, they **MUST** be tied to high or low.
3. The resistor, which connects to the FSADJ pin, is used for controlling the output maximum current of the DAC.

12 Package Information

12.1 KCD-A900-QA outline dimension

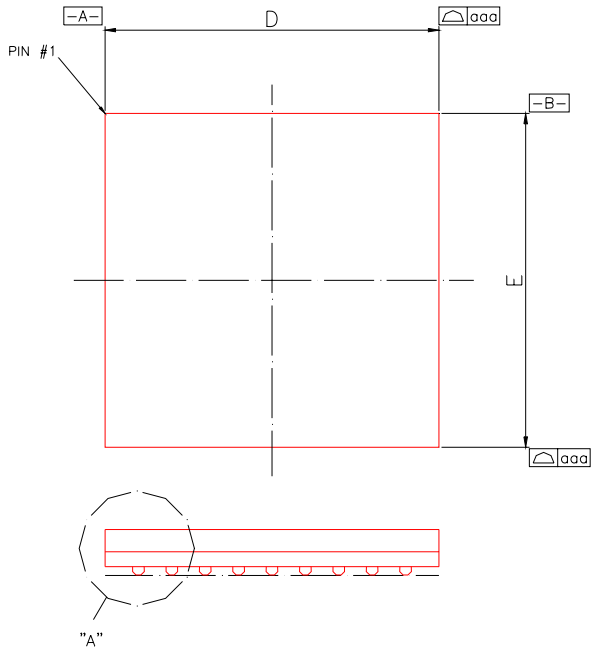


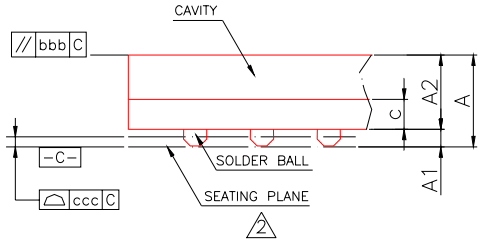
NOTE :

1. TO BE DETERMINED AT SEATING PLANE –C– .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS–026 , BDD.

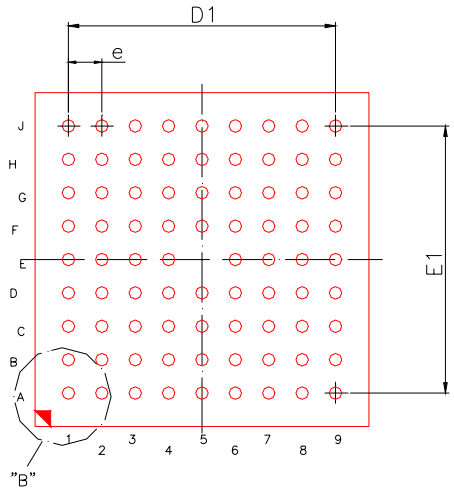
Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.20	0.27	0.007	0.008	0.011
b_1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	14.00 BSC			0.551 BSC		
D_1	12.00 BSC			0.472 BSC		
E	14.00 BSC			0.551 BSC		
E_1	12.00 BSC			0.472 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	0.15	—	0.003	0.006	—
R_2	0.15	0.20	0.25	0.006	0.008	0.010
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°

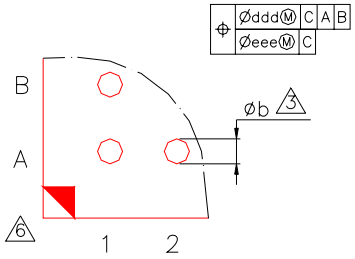
12.2 SSD1502G32 outline dimension





DETAIL : "A"





DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D1	---	6.40	---	---	0.252	---
E1	---	6.40	---	---	0.252	---
e	---	0.80	---	---	0.031	---
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.10			0.004		
bbb	0.20			0.008		
ccc	0.12			0.005		
ddd	0.15			0.006		
eee	0.08			0.003		
MD/ME	9/9			9/9		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-216
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY .