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CBM2090/CBM1190 Datasheet

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Contents

1 Description

Fastest & Securest USB 2.0/USB1.1 Flash Disk Controller with dedicated 32-bit microprocessor

The CBM2090 is the USB 2.0 Flash Disk controller with the fastest transfer speed on the market. CBM2090 can reach theoretical flash access speed limit of over 30MByte/s for read and 25MByte/s for write. For CBM1190, it can reach 1.0Mbytes/s write and 1.1Mbytes/s read.

The on-the-fly ECC engine is capable of correcting up to 4bytes (32bits), detect 5 or more bytes errors per 528bytes page . For data security, CBM2090/CBM1190 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

Each CBM2090/CBM1190 has its integrated Unique ID (UID). Thus greatly improved data security capability.

The CBM2090/CBM1190 supports all 8 bit and 16 bit NAND/MLC/AG-AND flash memory available in the market. New flash can be supported by software re-configuration. It also support up to 64MB Nor flash without extra components needed.

The CBM2090/CBM1190 has both a) 5V to 3.3V LDO and b) power on reset circuits integrated. Thus greatly reduced BOM cost and eased layout burden.

The USB2.0 flash disk controller CBM2090 is Pin to pin compatible with USB1.1 flash disk controller CBM1190, This enables the manufacturers to have the exactly same BOM and PCB layout for both USB1.1 and USB2.0 flash disk product.

The CBM2090/CBM1190 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, the CBM2090/CBM1190 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, disk partitions, password check for security disk, are available as part of our standard mass production software package.

The CBM2090/CBM1190 is available in 48-pin TQFP and 64-pin LQFP package, which are thinnest and smallest on the market. The 48-pin CBM2090/CBM1190 supports up to 4 flash chips and the 64-pin CBM2090L/CBM1190L supports up to 8 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

- **USB Interface**

  High-speed USB 2.0 interface; backward compatible with USB 1.1
  Integrated USB 2.0/USB1.1 PHY and controller

- **On-the-fly ECC built-in Hardware enhances reliability**

  ECC for Binary NAND flash: 4-32 bit/page (1 page = 528 bytes)
  ECC for MLC NAND flash: 8-32 bit/page
  ECC for AG-AND flash: 8-32 bit/page

- **Unique ID (UID) embeded.**

Greatly improved data security capability.

- **Hardware & Software Data Protection Technology**

  Prevent data corruption even if it is powered off or unplugged during data transfer.

- **NAND, AG-AND & MLC Flash Interface**

  Support 8-bit and 16-bit Samsung SLC and MLC NAND flash.
  Support 8-bit and 16-bit Toshiba SLC and MLC NAND flash.
  Support 8-bit and 16-bit Hynix SLC and MLC NAND flash.
  Support 8-bit and 16-bit ST Microelectronics SLC and MLC NAND flash.
  Support 8-bit and 16-bit Micron/IM SLC and MLC NAND flash.
  Support 8-bit and 16-bit Infenion SLC and MLC NAND flash.
  Support 8-bit and 16-bit Sandisk SLC and MLC NAND flash.
  Support Renesas AG-AND and AND flash memories
  Support Actrans flash memories
  Support up to 64MB Nor flash without extra components needed
  Software configuration to support various new flash memories
  Supports up to 8 flash chips.

- **Proprietary 32-bit CISC microprocessor feature**

  Proprietary 32-bit CISC processor for USB protocol processing and flash access.

  Single cycle instruction period

- **Integrated 5v to 3.3v voltage regulator**
- **Disk partitions and password check for security disk available**
- **PC boot up as USB Zip Disk, USB Hard Disk or CDRom**
- **Auto run function**
- **Low power dissipation**

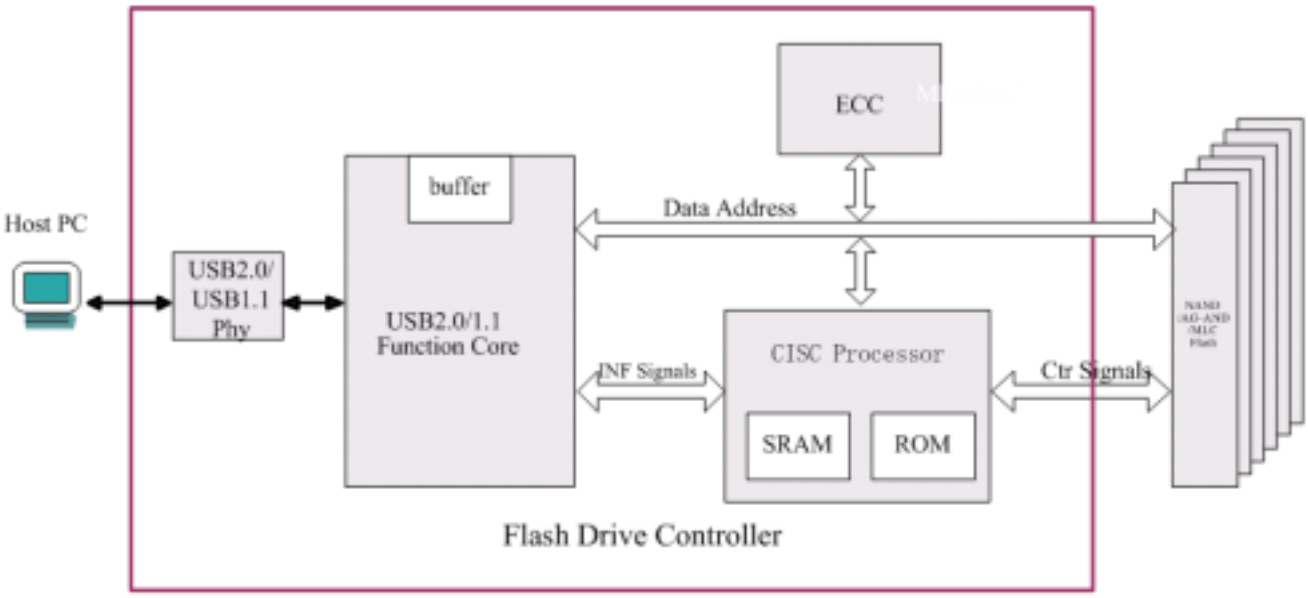
  Operating current 50mA (Bus power compatible)

- **Leading 0.18um CMOS technology**
- **48-pin TQFP /64-pin LQFP package**

  48-pin CBM2090/CBM1190 supports up to 4 Flash Chips
  64-pin CBM2090L/CBM1190L supports up to 8 Flash Chips

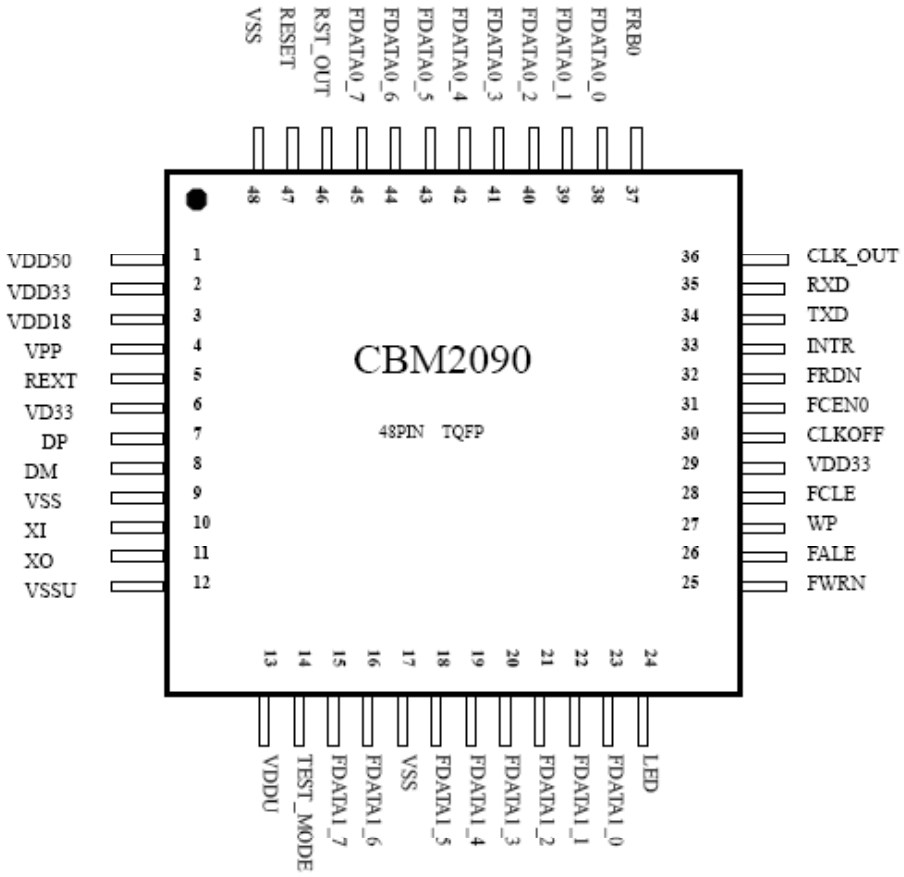
- **Windows, Mac and Linux compatible**

3 Block Diagram

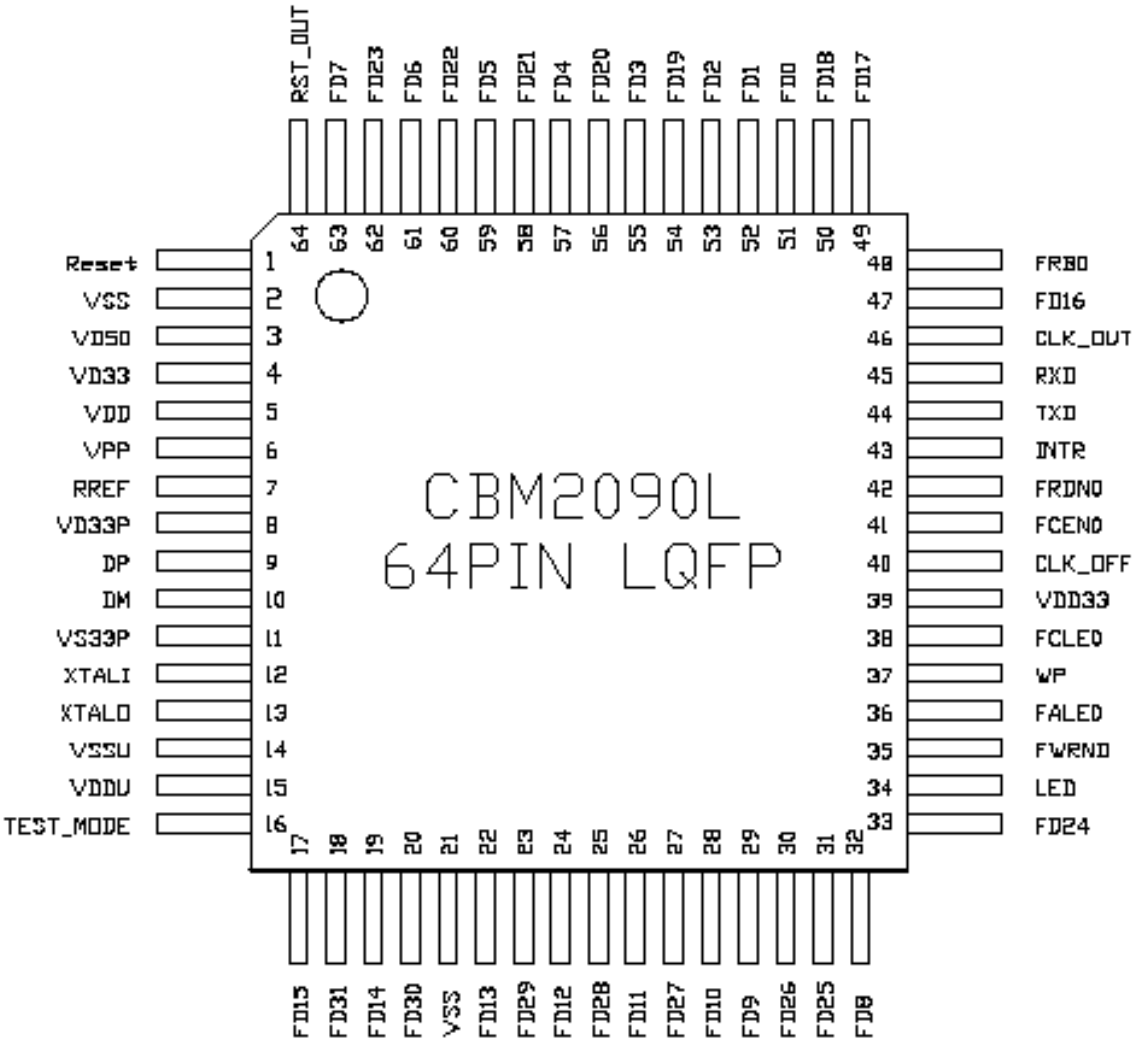


4 Pin Assignment

4.1 TQFP48 (Top Side)



4.2 LQFP64 (Top Side)



5 Pin Description

Brief CBM2090/CBM1190 pin functions are shown in the following tables.

I : Input signal

O : Output signal

I/O : Bi-direction signal

PWR : Power signal

GND: Ground signal

CBM2090 & CBM1190 LQFP64 / TQFP48 Pin Description

CBMXX90L LQFP64 Pin No.	CBMXX90/ CBM2078 TQFP48 Pin No.	Pin Name	Type	Description
		FCEN7	O	Flash Chip Enable - Chip 7 (active low)
	—	FCEN4	O	Flash Chip Enable - Chip 4 (active low)
	—	FCEN5	O	Flash Chip Enable - Chip 5(active low)
	—	FCEN3	O	Flash Chip Enable - Chip 3 (active low)
	—	FCEN6	O	Flash Chip Enable - Chip 6 (active low)
	—	FCEN2	O	Flash Chip Enable - Chip 2 (active low)
3	1	VDD50	PWR	Regulator5V Power Input
4	2	VDD33	PWR	Regulator 3.3V Power OUT
5	3	VDD18	PWR	Regulator 1.8V Out
6	4	VPP	I	Inner Programme
7	5	REXT	I	Connect External Resister for current reference
8	6	VD33	PWR	Padring 3.3V Power
9	7	DP	I/O	USB Data D+
10	8	DM	I/O	USB Data D-
2	9	VSS	GND	Padring 3.3V / Logic 1.8V Ground
12	10	XI	I	Crystal Input (12 MHz)
13	11	XO	O	Crystal Output
14	12	VSSU	GND	Analog 1.8V Ground
15	13	VDDU	PWR	Analog 1.8V Power

16	14	TEST_MODE	I	Test Mode Enable Pin
17	15	FDATA1_7 GPIO15	I/O	Group 1 Flash Data Bus - bit 7 General I/O port 15
19	16	FDATA1_6 GPIO14	I/O	Group 1 Flash Data Bus - bit 6 General I/O port 14
21	17	VSS	GND	Padring 3.3V / Logic 1.8V Ground
22	18	FDATA1_5 GPIO13	I/O	Group 1 Flash Data Bus - bit 5 General I/O port 13
24	19	FDATA1_4 GPIO12	I/O	Group 1 Flash Data Bus - bit 4 General I/O port 12
26	20	FDATA1_3 GPIO11	I/O	Group 1 Flash Data Bus - bit 3 General I/O port 11
28	21	FDATA1_2 GPIO10	I/O	Group 1 Flash Data Bus - bit 2 General I/O port 10
29	22	FDATA1_1 GPIO9	I/O	Group 1 Flash Data Bus - bit 1 General I/O port 9
32	23	FDATA1_0 GPIO8	I/O	Group 1 Flash Data Bus - bit 0 General I/O port 8
34	24	LED	O	LED Indication
35	25	FWRN	O	Group Flash Write Enable (active low)
36	26	FALE	O	Group Flash Address Latch Enable
37	27	WP	I	Write Protect Switch Input
38	28	FCLE	O	Group Flash Command Latch Enable
39	29	VDD33	PWR	Padring 3.3V Power
40	30	CLKOFF	O	Clock output switch
41	31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
42	32	FRDN	O	Group Flash Read Enable (active low)
43	33	FRB1	I	Group Flash Ready_Busy
44	34	TXD	O	Serial port data out
45	35	RXD	I	Serial port data in
46	36	FCEN1	O	Flash Chip Enable - Chip 1
48	37	FRB0	I	Group Flash Ready_Busy
51	38	FDATA0_0 GPIO0	I/O	Group 0 Flash Data Bus - bit 0 General I/O port 0
52	39	FDATA0_1 GPIO1	I/O	Group 0 Flash Data Bus - bit 1 General I/O port 1
53	40	FDATA0_2 GPIO2	I/O	Group 0 Flash Data Bus - bit 2 General I/O port 2
55	41	FDATA0_3 GPIO3	I/O	Group 0 Flash Data Bus - bit 3 General I/O port 3
57	42	FDATA0_4 GPIO4	I/O	Group 0 Flash Data Bus - bit 4 General I/O port 4

59	43	FDATA0_5 GPIO5	I/O	Group 0 Flash Data Bus - bit 5 General I/O port 5
61	44	FDATA0_6 GPIO6	I/O	Group 0 Flash Data Bus - bit 6 General I/O port 6
63	45	FDATA0_7 GPIO7	I/O	Group 0 Flash Data Bus - bit 7 General I/O port 7
64	46	RST_OUT	O	Chip reset output/ External device reset signal
1	47	RESET	I	Reset Sign (active low)
8	48	VS33A	GND	Analog 3.3V Ground
47		FDATA2_0	I/O	Group 2 Flash Data Bus - bit 0 General I/O port
49		FDATA2_1	I/O	Group2 Flash Data Bus - bit 1 General I/O port
50		FDATA2_2	I/O	Group 2 Flash Data Bus - bit 2 General I/O port
54		FDATA2_3	I/O	Group 2 Flash Data Bus - bit 3 General I/O port
56		FDATA2_4	I/O	Group 2 Flash Data Bus - bit 4 General I/O port
58		FDATA2_5	I/O	Group2 Flash Data Bus - bit 5 General I/O port
60		FDATA2_6	I/O	Group 2 Flash Data Bus - bit 6 General I/O port
62		FDATA2_7	I/O	Group 2 Flash Data Bus - bit 7 General I/O port
33		FDATA3_0	I/O	Group 3 Flash Data Bus - bit 0 General I/O port
31		FDATA3_1	I/O	Group 3 Flash Data Bus - bit 1 General I/O port
30		FDATA3_2	I/O	Group 3 Flash Data Bus - bit 2 General I/O port
27		FDATA3_3	I/O	Group 3 Flash Data Bus - bit 3 General I/O port
25		FDATA3_4	I/O	Group 3 Flash Data Bus - bit 4 General I/O port
23		FDATA3_5	I/O	Group 3 Flash Data Bus - bit 5 General I/O port
20		FDATA3_6	I/O	Group3 Flash Data Bus - bit 6 General I/O port
18		FDATA3_7	I/O	Group 3 Flash Data Bus - bit 7 General I/O port

6 Electrical Characteristics

6.1 ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VCCA	analog supply voltage			-0.5	5.5	v
VCCD	digital supply voltage			-0.5	4.5	v
VI	input voltage			-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	DP, DM and GND pins	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	℃

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k . resistor (Human Body Model).

6.2 RECOMMENDED OPERATING CONDITIONS

symbol	Parameter	conditions	min	Typ	max	Unit
VCCA	analog supply voltage		3.0	3.3	3.6	V
VCCD	digital supply voltage		3.0	3.3	3.6	V
VI	input voltage		0	-	VCCD	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	℃

6.3 STATIC CHARACTERISTICS

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = 40 to 85 ℃;

symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode	-	500		uA

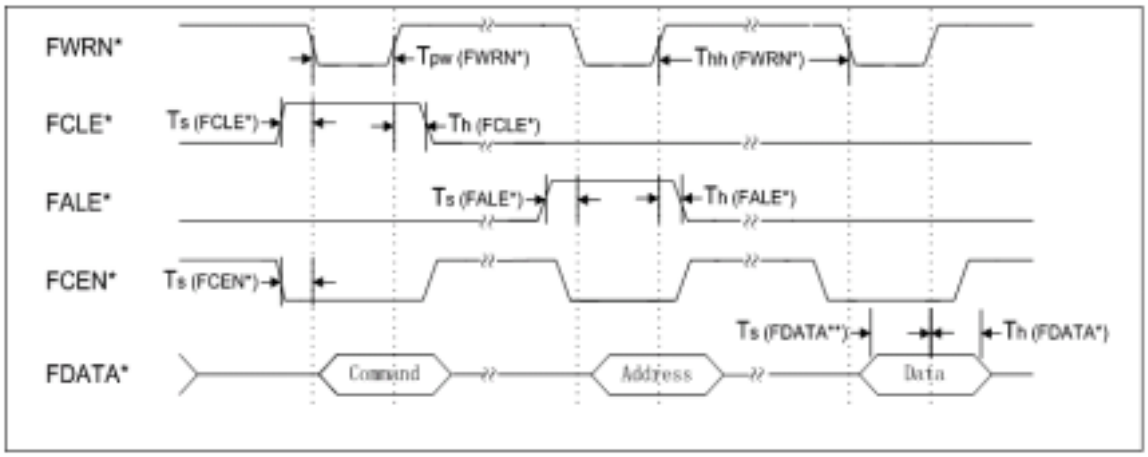
6.4 DYNAMIC CHARACTERISTICS

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = 40 to 85 ℃ ;

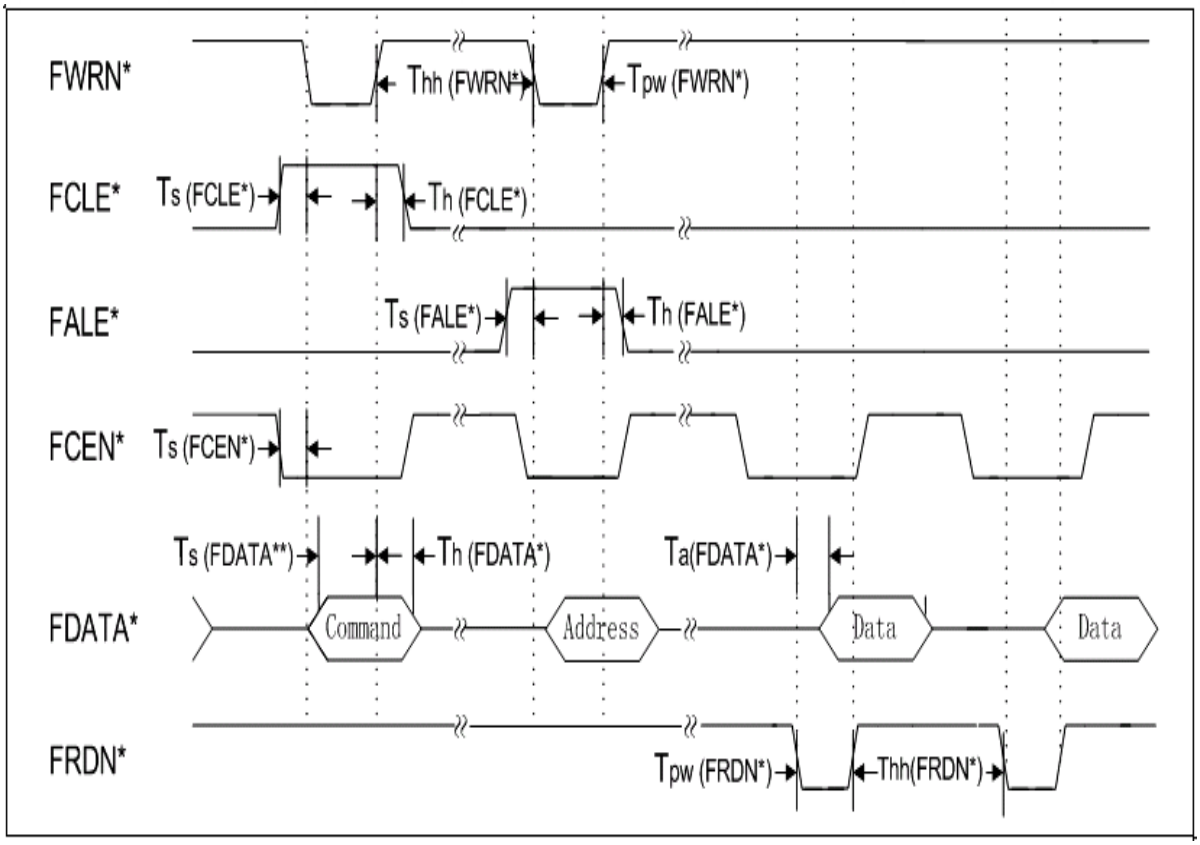
symbol	Parameter	conditions	min	Typ	max	Unit

Ts(FDATA*)	FDATA* setup time relative to rising FWRN* edge		-	33	-	ns
Th(FDATA*)	FDATA* hold time relative to falling FWRN* edge		-	33	-	ns
Ts (FCLE*)	FCLE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FCLE*)	FCLE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FALE*)	FALE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FALE*)	FALE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FCEN*)	FCEN* setup time relative to falling FWRN* edge		-	99	-	ns
Tpw (FWRN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FWRN*)	FWRN* high hold time		-	33	-	ns
Ta(FDATA*)	FDATA* access time relative to falling FRDN* edge		-	-	40	ns
Tpw (FRDN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FRDN*)	FWRN* high hold time		-	33	-	ns

Timing diagram for Writing of Data



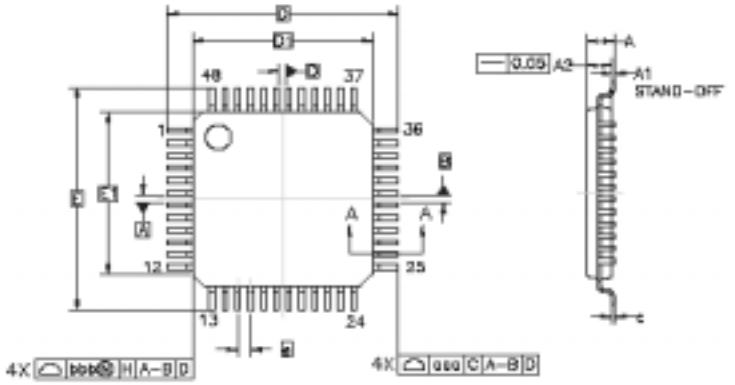
Timing diagram for Reading of Data

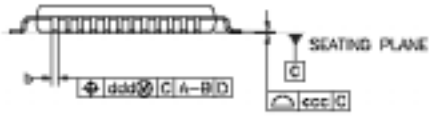

FWRN*
Thh (FWRN*)
Tpw (FWRN*)
FCLE*
Ts (FCLE*)
Th (FCLE*)
FALE*
Ts (FALE*)
Th (FALE*)
FCEN*
Ts (FCEN*)
Ts (FDATA**)
Th (FDATA*)
Ta(FDATA*)
FDATA*
Command
Address
Data
Data
FRDN*
Tpw (FRDN*)
Thh(FRDN*)

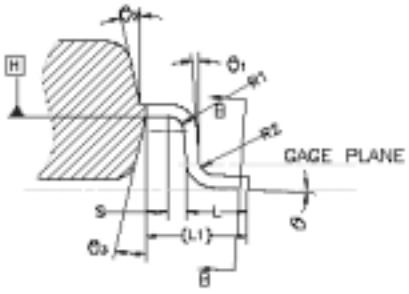
7 Mechanical Dimensions

7.1 48-Pin CBM2090/CBM1190 Package Outline Dimension

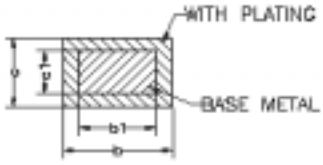
DOC No.: 0048-TQ7.0X7.0-01-A







SECTION A–A



SECTION B–B

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
eee	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H;
3. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONTION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;
4. DIMENSION A INCLUDES STANDOFF HEIGHT A1,PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES;
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TQFP 7.0 × 7.0 mm 48L Package Outline Dimension

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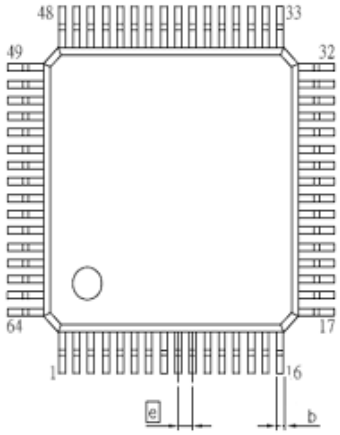
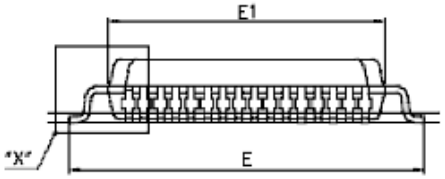
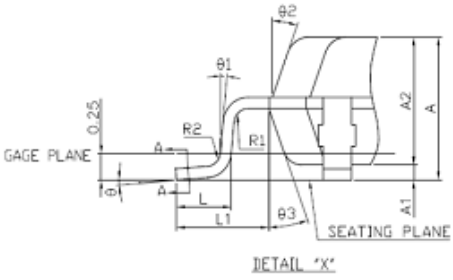
7.2 64-Pin CBM2090/CBM1190 Package Outline Dimension

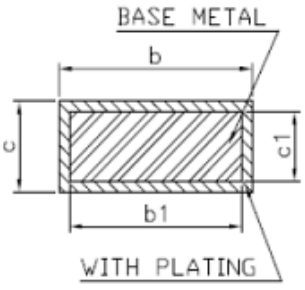
DOC No.: 0064-7.0X7.0-01-A



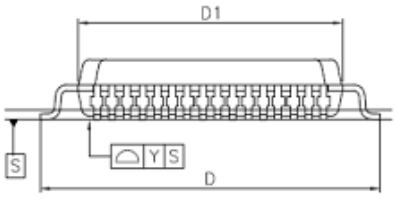




DETAIL "X"



SECTION A-A



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.40 BSC			15.8 BSC		
L	0.45	0.60	0.75	18	24	30
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1. REFER TO JEDEC MS-026(ISSUE C)/BBD
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4. ALL DIMENSIONS IN MILLIMETERS.

LQFP 7.0×7.0 mm 64L Package

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