Datasheet

SiRFatlasIV
AT8401 Series Application Processor

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OVERVIEW

The SiRFatlasIV™ processor is the next generation in high performance and low cost navigation. Using advanced process technology and with a large number of hardware accelerators, SiRFatlasIV provides better system and GPS performances with a high-speed ARM®-1136 RISC processor core and a 16-bit DSP core. This state-of-the-art processor supports GPS baseband and higher bandwidth SDRAM memory controllers, offering powerful solutions for performance-intense navigation, multimedia and graphics applications.

FEATURES

- 500MHz 32-bit RISC (ARM1136)
  - 16KB I-Cache
  - 16KB D-Cache
  - 16KB D-TCM
  - 16KB I-TCM
  - Low Power advanced 65nm process
- 250MHz 16-bit DSP
  - With high performance hardware FFT
  - Hardware Energy Peak Detection (EPD)
  - Idle mode
  - 12Kx24bit program memory
  - 20Kx16bit data memory
- Memory controller support:
  - 1.8V 333MHz Mobile-DDR
  - 2.5V 32-bit 400MHz DDR1
  - Max. size 128MB
- 64-channel GPS baseband with hardware match filter
- USB-2.0 Hi-Speed controller
  - USB 2.0 High-Speed On-The-Go (OTG) controller serves as either a USB Host or a USB Device controller with on-chip PHY
- 8-bit NAND Flash interface
  - 8-bit BCH Hardware ECC by 512 byte
  - Direct boot from SLC or MLC NAND Flash
  - Supports page size 512 byte, 2k byte, and 4k byte
- 8/16-bit Async-ROM interface for CPU interface LCD
  - One address line
  - FIFO mode operation
- 4-slot SD/SDIO/MMC+ controller
  - Direct boot from SD/MMC+ Managed NAND
  - Four SDHC/SD 2.0/MMC4.2 ports
  - SDIO support for WiFi, Bluetooth, and DVB-T/DVB-H/T-DMB/S-DMB
- 8/16-bit LCD interface
- Video input port
  - 8/10-bit
  - Raw RGB, RGB, YUV data format
  - CCIR-601
  - CCIR-656
- Audio CODEC interface
  - AC97 V2.2 standard
  - I^2S master/slave mode
- One SPI port
- Two Universal Serial Ports (USP)
- Two UART ports
- Two I^2C ports
- Four PWM pins
- 12mmx12mm, 0.65mm pitch, 292-pin TFBGA package

BLOCK DIAGRAM

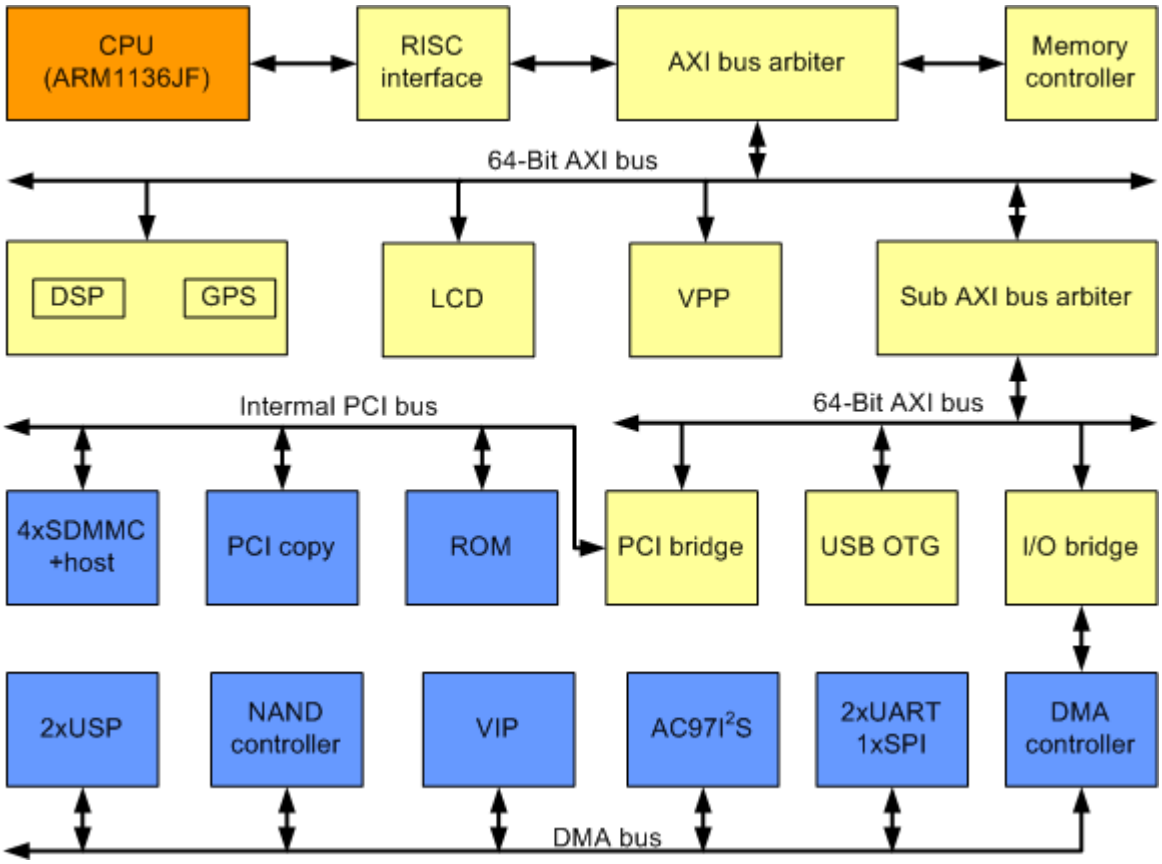


Figure 1: SiRFatlasIV Block Diagram

PACKAGE AND PIN SPECIFICATION

Mechanical Drawing of Package

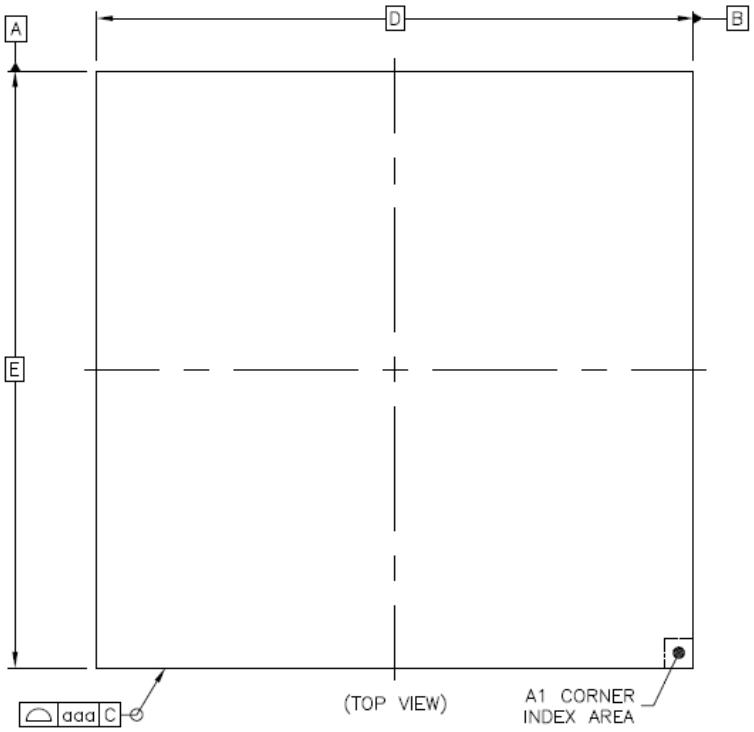


Figure 2: Top View

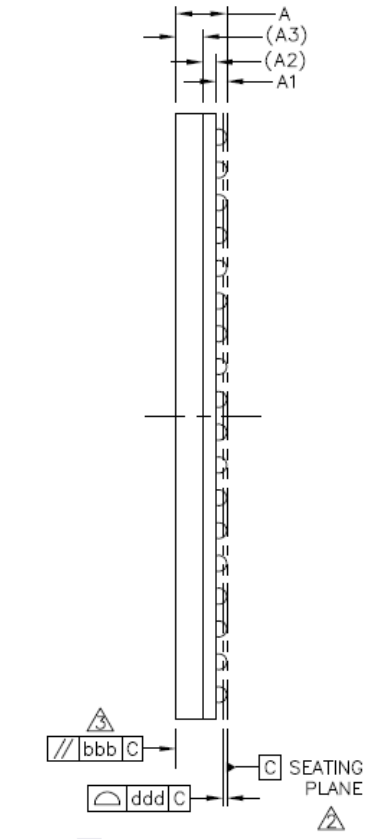


Figure 3: Side View

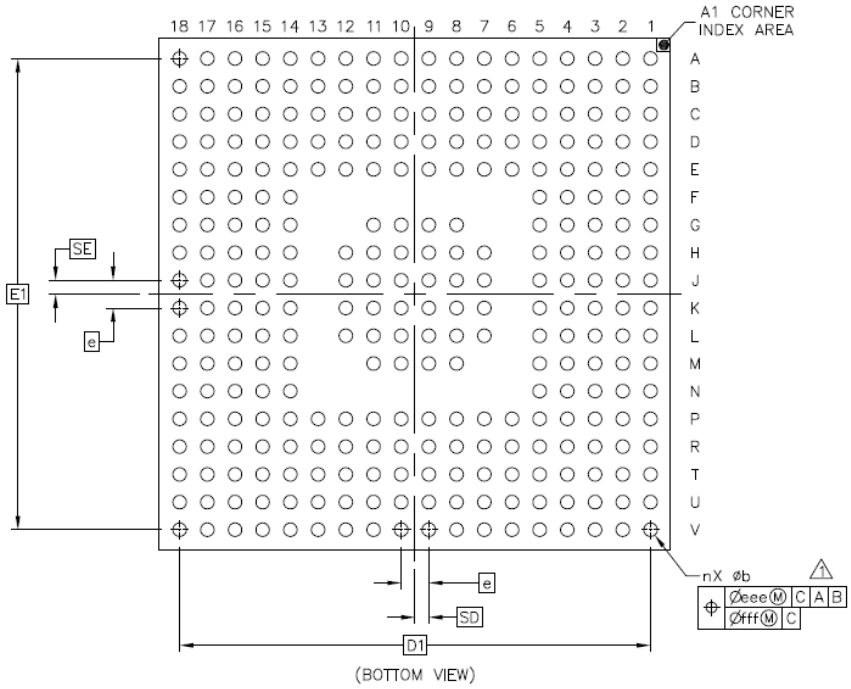


Figure 4: Bottom View

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.1
STAND OFF	A1	0.16	---	0.26
SUBSTRATE THICKNESS	A2		0.26	REF
MOLD THICKNESS	A3		0.54	REF
BODY SIZE	D		12	BSC
	E		12	BSC
BALL DIAMETER			0.3	
BALL OPENING			0.275	
BALL WIDTH	b	0.27	---	0.37
BALL PITCH	e		0.65	BSC
BALL COUNT	n		292	
EDGE BALL CENTER TO CENTER	D1		11.05	BSC
	E1		11.05	BSC
BODY CENTER TO CONTACT BALL	SD		0.325	BSC
	SE		0.325	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.2	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT

Figure 5: Notes for Package Information

Pin Sequence and Ball Assignment

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_DF_RE_B	VDDIO_Nand	PDB08DGZ	Decided by boot mode	O(H):Nand/I(Z):SD	Programmable
X_DF_RY_BY	VDDIO_Nand	PDUSDGZ	NAND	I(U)	I(U)
X_DF_WP_B	VDDIO_Nand	PDB08DGZ	NAND	O(L)	Programmable
X_DF_CS_B[1]	VDDIO_Nand	PDO04CDG	NAND	O(H)	Programmable
X_DF_CS_B[0]	VDDIO_Nand	PDO04CDG	NAND	O(H)	Programmable
X_L_PCLK	VDDIO_LCD	PDD08SDGZ	LCD	I(D)	Programmable
X_L_LCK	VDDIO_LCD	PDD08SDGZ	LCD	I(D)	Programmable
X_L_FCK	VDDIO_LCD	PDD08SDGZ	LCD	I(D)	Programmable
X_L_DE	VDDIO_LCD	PDDW04DGZ	GPIO	I(D)	Programmable
X_LDD[0]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[1]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[2]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[3]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[4]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[5]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[6]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[7]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[8]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[9]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[10]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_LDD[11]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[12]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[13]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[14]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_LDD[15]	VDDIO_LCD	PDB04DGZ	LCD	O(L)	O(L)
X_GPS_SGN	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_GPS_MAG	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_GPS_SAMPLE_CLK	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_GPS_CLK	VDDIO	PDB04SDGZ	GPS	I(Z)	Programmable
X_GPIO[0]	VDDIO	PDU04SDGZ	GPIO	I(U)	Programmable /wakeup
X_GPIO[1]	VDDIO	PDU04SDGZ	GPIO	I(U)	Programmable /wakeup
X_GPIO[2]	VDDIO	PDB08SDGZ	GPIO	I(Z)	Programmable /wakeup
X_GPIO[3]	VDDIO	PDB08SDGZ	GPIO	I(Z)	Programmable /wakeup
X_SD_CD_B_1	VDDIO	PDUW04DGZ	GPIO	I(U)	Programmable
X_SD_VCC_ON_1	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_SD_WP_B_1	VDDIO	PDUW04DGZ	GPIO	I(U)	Programmable
X_SD_CLK_1	VDDIO	PDUW16DGZ	GPIO	I(U)	Programmable
X_SD_CMD_1	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_1[0]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_1[1]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_SD_DAT_1[2]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_1[3]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_CLK_3	VDDIO	PDUW16DGZ	GPIO	I(U)	Programmable
X_SD_CMD_3	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_3[0]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_3[1]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_3[2]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_SD_DAT_3[3]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable
X_CKO_1	VDDIO	PDDW08DGZ	GPIO	I(D)	Programmable
X_AC97_BIT_CLK	VDDIO	PDD04SDGZ	AC97	I(D)	Programmable
X_AC97_DOUT	VDDIO	PDDW04DGZ	AC97	O(L)	Programmable
X_AC97_DIN	VDDIO	PDDW04DGZ	AC97	I(D)	Programmable
X_AC97_SYNC	VDDIO	PDD04DGZ	AC97	O(L)	Programmable
X_TXD_0	VDDIO	PDT04DGZ	UART	O(H)	I(Z)
X_RXD_0	VDDIO	PDUW04DGZ	UART	I(U)	Programmable
X_TXD_1	VDDIO	PDT04DGZ	UART	O(H)	I(Z)
X_RXD_1	VDDIO	PDUW04DGZ	UART	I(U)	Programmable
X_USCLK_0	VDDIO	PDD08SDGZ	GPIO	I(D)	Programmable
X_UTXD_0	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_URXD_0	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_UTFS_0	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_URFS_0	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_USCLK_1	VDDIO	PDD08SDGZ	GPIO	I(D)	Programmable
X_UTXD_1	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_URXD_1	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_UTFS_1	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_URFS_1	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_PWR_EN	VDDIO	PDO08CDG	-	O(H)	O(L)
X_USB_VBUS	VDDA3V3_USB	PDBANA_5VT	-	-	-
X_USB_ID	VDDA3V3_USB	PDB3A_USB	-	-	-
X_USB_DN	VDDA3V3_USB	PDBANA_5VT	-	-	-
X_USB_DP	VDDA3V3_USB	PDBANA_5VT	-	-	-
X_USB_RREFEXT	VDDA3V3_USB	PDB3A_USB	-	-	-
X_USB_TEST_GPANAIO	VDDA3V3_USB	PDB3A_USB	-	-	-
X_XINW	VDDIO_RTC	PDXO01M_GUC_65LP	-	-	-
X_XOUTW	VDDIO_RTC		-	-	-
X_RESET_B	VDDIO_RTC	PDISDGZ	-	I(U)	I(U)
X_TEST_MODE[5]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)
X_TEST_MODE[4]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)
X_TEST_MODE[3]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_TEST_MODE[2]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)
X_TEST_MODE[1]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)
X_TEST_MODE[0]	VDDIO_RTC	PDIDGZ	-	I(Z)	I(Z)
X_ALARM_WAKEUP	VDDIO_RTC	PDO08CDG	-	O(L)	O(L)
X_XIN	VDDIO	PDXOE3DG	-	-	-
X_XOUT	VDDIO		-	-	-
X_SCAN_EN	VDDIO	PDDDGZ	-	I(D)	I(D)
X_CKO_0	VDDIO	PDO08CDG	-	O(L)	O(L)
X_GPIO[4]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable /wakeup
X_GPIO[5]	VDDIO	PDUW08DGZ	GPIO	I(U)	Programmable /wakeup
X_GPIO[6]	VDDIO	PDDW08DGZ	GPIO	I(D)	Programmable /wakeup
X_GPIO[7]	VDDIO	PDDW08DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[9]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[8]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[7]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[6]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[5]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[4]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[3]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[2]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_VIP_PXD[1]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_PXD[0]	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable /wakeup
X_VIP_VSYNC	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_VIP_HSYNC	VDDIO	PDDW04DGZ	GPIO	I(D)	Programmable
X_VIP_PXCLK	VDDIO	PDD04SDGZ	GPIO	I(D)	Programmable
X_CPH_CLK	VDDIO	PDD08SDGZ	GPIO	I(D)	Programmable
X_CPH_FS_CLK	VDDIO	PDD08SDGZ	GPIO	I(D)	Programmable
X_GPIO[8]	VDDIO	PDU04SDGZ	GPIO	I(U)	Programmable /wakeup
X_GPIO[9]	VDDIO	PDUW04DGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[10]	VDDIO	PDUW04DGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[11]	VDDIO	PDUW04DGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[12]	VDDIO	PDU04SDGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[13]	VDDIO	PDU04SDGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[14]	VDDIO	PDU04SDGZ	Decided by boot mode	I(U)	Programmable /wakeup
X_GPIO[15]	VDDIO	PDD04SDGZ	Decided by boot mode	I(D)	Programmable /wakeup
X_SDA_0	VDDIO	PDB08SDGZ	GPIO	I(Z)	Programmable
X_SCL_0	VDDIO	PDB08SDGZ	GPIO	I(Z)	Programmable
X_XP	VDDA_TSC	PDB3A	-	-	-
X_XN	VDDA_TSC	PDB3A	-	-	-
X_YP	VDDA_TSC	PDB3A	-	-	-
X_YN	VDDA_TSC	PDB3A	-	-	-
VREF_ADC	VDDA_TSC	PDB3A	-	-	-

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_AUX0	VDDA_TSC	PDB3A	-	-	-
X_AUX1	VDDA_TSC	PDB3A	-	-	-
X_AUX2	VDDA_TSC	PDB3A	-	-	-
X_MCKE	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MCS_B	VDDIO_MEM	PMEMIO	-	O(H)	Programmable
X_MWE_B	VDDIO_MEM	PMEMIO	-	O(H)	Programmable
X_MRAS_B	VDDIO_MEM	PMEMIO	-	O(H)	Programmable
X_MCAS_B	VDDIO_MEM	PMEMIO	-	O(H)	Programmable
X_MD[31]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[30]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[29]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[28]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MDQM[3]	VDDIO_MEM	PMEMIO	-	O(H)	O(L)
X_MDQS[3]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[27]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[26]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[25]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[24]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[23]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[22]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[21]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[20]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MDQM[2]	VDDIO_MEM	PMEMIO	-	O(H)	O(L)
X_MDQS[2]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[19]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[18]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[17]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[16]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[15]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_MD[14]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[13]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[12]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MDQM[1]	VDDIO_MEM	PMEMIO	-	O(H)	O(L)
X_MDQS[1]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[11]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[10]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[9]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[8]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[7]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[6]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[5]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[4]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MDQM[0]	VDDIO_MEM	PMEMIO	-	O(H)	O(L)
X_MDQS[0]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[3]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[2]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[1]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MD[0]	VDDIO_MEM	PMEMIO	-	I(Z)	O(L)
X_MCLK_O	VDDIO_MEM	PMEMIODIF	-	O(CLK)	Programmable
X_MCLKB_O	VDDIO_MEM		-	O(CLK)	Programmable
X_M_BA[1]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_M_BA[0]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[12]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[11]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[10]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[9]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)

Pin Name	I/O Power	Pad Cell	Default Function	Reset State	Sleep State
X_MA[8]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[7]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[6]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[5]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[4]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[3]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[2]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[1]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_MA[0]	VDDIO_MEM	PMEMIO	-	O(L)	O(L)
X_DF_AD[7]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[6]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[5]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[4]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[3]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[2]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[1]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_AD[0]	VDDIO_Nand	PDDW08DGZ	Decided by boot mode	I (Z): NAND/ I (Z): SD	Programmable
X_DF_CLE	VDDIO_Nand	PDB08DGZ	Decided by boot mode	O(L): Nand O(L): SD	Programmable
X_DF_ALE	VDDIO_Nand	PDB08DGZ	Decided by boot mode	O(L): Nand I(Z): SD	Programmable
X_DF_WE_B	VDDIO_Nand	PDB08DGZ	Decided by boot mode	O(H): Nand O(L): SD	Programmable

Table 1: Pin Status

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_DF_RE_B	DF_RE_B	SD_CMD_2	-	-	PWR_PROG[120]
X_DF_RY_BY	DF_RY_BY		-	-	FIX
X_DF_WP_B	DF_WP_B	SD_VCC_ON_0	-	-	PWR_PROG[131]
X_DF_CS_B[1]	DF_CS_B[3]		-	-	PWR_PROG[108]
X_DF_CS_B[0]	DF_CS_B[0]	DF_CS_B[2]	-	-	PWR_PROG[109]
X_L_PCLK	L_PCLK	FCE_B[1]	-	-	PWR_PROG[6]
X_L_LCK	L_LCK	FWE_B	-	-	PWR_PROG[141]
X_L_FCK	L_FCK	FOE_B	-	-	PWR_PROG[142]
X_L_DE	L_DE	FA[1]	-	GPIO3[23]	PWR_PROG[143]
X_LDD[0]	LDD[0]	FD[0]	-	-	FIX
X_LDD[1]	LDD[1]	FD[1]	-	-	FIX
X_LDD[2]	LDD[2]	FD[2]	-	-	FIX
X_LDD[3]	LDD[3]	FD[3]	-	-	FIX
X_LDD[4]	LDD[4]	FD[4]	-	-	FIX
X_LDD[5]	LDD[5]	FD[5]	-	-	FIX
X_LDD[6]	LDD[6]	FD[6]	-	-	FIX
X_LDD[7]	LDD[7]	FD[7]	-	-	FIX
X_LDD[8]	LDD[8]	FD[8]	-	-	FIX
X_LDD[9]	LDD[9]	FD[9]	-	-	FIX
X_LDD[10]	LDD[10]	FD[10]	-	-	FIX
X_LDD[11]	LDD[11]	FD[11]	-	-	FIX
X_LDD[12]	LDD[12]	FD[12]	-	-	FIX
X_LDD[13]	LDD[13]	FD[13]	-	-	FIX
X_LDD[14]	LDD[14]	FD[14]	-	-	FIX
X_LDD[15]	LDD[15]	FD[15]	-	-	FIX
X_GPS_SGN	GPS_SGN	-	-	GPIO3[20]	PWR_PROG[2]

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_GPS_MAG	GPS_MAG	-	-	GPIO3[21]	PWR_PROG[3]
X_GPS_SAMPLE_CLK	GPS_SAMPLE_CLK	-	-	GPIO3[22]	PWR_PROG[4]
X_GPS_CLK	GPS_CLK	-	-	GPIO4[28]	PWR_PROG[5]
X_GPIO[0]	-	-	-	GPIO0[0]	PWR_PROG[23]
X_GPIO[1]	-	-	-	GPIO0[1]	PWR_PROG[24]
X_GPIO[2]	SCL_1	-	-	GPIO0[2]	PWR_PROG[25]
X_GPIO[3]	SDA_1	-	-	GPIO0[3]	PWR_PROG[26]
X_SD_CD_B_1	SD_CD_B_1	-	-	GPIO1[7]	PWR_PROG[62]
X_SD_VCC_ON_1	SD_VCC_ON_1	-	-	GPIO1[8]	PWR_PROG[63]
X_SD_WP_B_1	SD_WP_B_1	-	-	GPIO1[9]	PWR_PROG[64]
X_SD_CLK_1	SD_CLK_1	-	-	GPIO1[10]	PWR_PROG[65]
X_SD_CMD_1	SD_CMD_1	-	-	GPIO1[11]	PWR_PROG[66]
X_SD_DAT_1[0]	SD_DAT_1[0]	-	-	GPIO1[12]	PWR_PROG[67]
X_SD_DAT_1[1]	SD_DAT_1[1]	-	-	GPIO1[13]	PWR_PROG[144]
X_SD_DAT_1[2]	SD_DAT_1[2]	-	-	GPIO1[14]	PWR_PROG[145]
X_SD_DAT_1[3]	SD_DAT_1[3]	-	-	GPIO1[15]	PWR_PROG[146]
X_SD_CLK_3	SD_CLK_3	-	-	GPIO1[2]	PWR_PROG[121]
X_SD_CMD_3	SD_CMD_3	-	-	GPIO1[3]	PWR_PROG[122]
X_SD_DAT_3[0]	SD_DAT_3[0]	SPI_EN_0	-	GPIO1[28]	PWR_PROG[123]
X_SD_DAT_3[1]	SD_DAT_3[1]	SPI_CLK_0	-	GPIO1[29]	PWR_PROG[124]
X_SD_DAT_3[2]	SD_DAT_3[2]	SPI_DIN_0	-	GPIO1[0]	PWR_PROG[125]

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_SD_DAT_3[3]	SD_DAT_3[3]	SPI_DOUT_0	-	GPIO1[1]	PWR_PROG[126]
X_CKO_1	CKO_1	I2S_MCLK	-	GPIO1[20]	PWR_PROG[68]
X_AC97_BIT_CLK	AC97_BIT_CLK	I2S_BCLK	-	-	PWR_PROG[127]
X_AC97_DOUT	AC97_DOUT	I2S_DOUT[0]	-	-	PWR_PROG[128]
X_AC97_DIN	AC97_DIN	I2S_DIN	-	-	PWR_PROG[129]
X_AC97_SYNC	AC97_SYNC	I2S_LRCLK	-	-	PWR_PROG[130]
X_TXD_0	TXD_0	-	-	-	FIX
X_RXD_0	RXD_0	-	-	GPIO3[15]	PWR_PROG[118]
X_TXD_1	TXD_1	-	-	-	FIX
X_RXD_1	RXD_1	-	-	GPIO3[16]	PWR_PROG[119]
X_USCLK_0	USCLK_0	I2S_EXTCLK	-	GPIO0[18]	PWR_PROG[41]
X_UTXD_0	UTXD_0	-	-	GPIO0[19]	PWR_PROG[42]
X_URXD_0	URXD_0	-	-	GPIO0[20]	PWR_PROG[43]
X_UTFS_0	UTFS_0	USB1_UTMI_DRVVBUS	-	GPIO0[21]	PWR_PROG[44]
X_URFS_0	URFS_0	I2S_DOUT[1]	RTS_0	GPIO0[22]	PWR_PROG[45]
X_USCLK_1	USCLK_1	-	-	GPIO0[23]	PWR_PROG[46]
X_UTXD_1	UTXD_1	-	-	GPIO0[24]	PWR_PROG[47]
X_URXD_1	URXD_1	-	-	GPIO0[25]	PWR_PROG[48]
X_UTFS_1	UTFS_1	-	-	GPIO0[26]	PWR_PROG[49]
X_URFS_1	URFS_1	I2S_DOUT[2]	CTS_0	GPIO0[27]	PWR_PROG[50]
X_PWR_EN	PWR_EN	-	-	-	-

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_USB_VBUS	-	-	-	-	-
X_USB_ID	-	-	-	-	-
X_USB_DN	-	-	-	-	-
X_USB_DP	-	-	-	-	-
X_USB_RREFEXT	-	-	-	-	-
X_USB_TEST_GPANAIO	-	-	-	-	-
X_XINW	XINW	-	-	-	-
X_XOUTW		-	-	-	-
X_RESET_B	RESET_B	-	-	-	-
X_TEST_MODE[5]	TEST_MODE[5]	-	-	-	-
X_TEST_MODE[4]	TEST_MODE[4]	-	-	-	-
X_TEST_MODE[3]	TEST_MODE[3]	-	-	-	-
X_TEST_MODE[2]	TEST_MODE[2]	-	-	-	-
X_TEST_MODE[1]	TEST_MODE[1]	-	-	-	-
X_TEST_MODE[0]	TEST_MODE[0]	-	-	-	-
X_ALARM_WAKEUP	ALARM_WAKEUP	-	-	-	-
X_XIN	XIN	-	-	-	-
X_XOUT	-	-	-	-	-
X_SCAN_EN	SCAN_EN	-	-	-	-
X_CKO_0[1]	CKO_0	-	-	-	FIX
X_GPIO[4]	PWM0	GPS_START	-	GPIO0[4]	PWR_PROG[27]
X_GPIO[5]	PWM1	GPS_STOP	-	GPIO0[5]	PWR_PROG[28]

[1] This pad can be used to output XIN or XINW. Refer to the register description of PWR_CTRL in the chapter of Power Management.

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_GPIO[6]	PWM2	GPS_INT	-	GPIO0[6]	PWR_PROG[29]
X_GPIO[7]	PWM3	-	-	GPIO0[7]	PWR_PROG[30]
X_VIP_PXD[9]	VIP_PXD[9]	-	-	GPIO4[6]	PWR_PROG[15]
X_VIP_PXD[8]	VIP_PXD[8]	-	-	GPIO4[7]	PWR_PROG[16]
X_VIP_PXD[7]	VIP_PXD[7]	-	-	GPIO4[8]	PWR_PROG[17]
X_VIP_PXD[6]	VIP_PXD[6]	-	-	GPIO4[9]	PWR_PROG[134]
X_VIP_PXD[5]	VIP_PXD[5]	-	-	GPIO4[10]	PWR_PROG[135]
X_VIP_PXD[4]	VIP_PXD[4]	-	-	GPIO4[11]	PWR_PROG[136]
X_VIP_PXD[3]	VIP_PXD[3]	-	-	GPIO4[12]	PWR_PROG[137]
X_VIP_PXD[2]	VIP_PXD[2]	-	-	GPIO4[13]	PWR_PROG[138]
X_VIP_PXD[1]	VIP_PXD[1]	-	-	GPIO4[14]	PWR_PROG[139]
X_VIP_PXD[0]	VIP_PXD[0]	-	-	GPIO4[15]	PWR_PROG[140]
X_VIP_VSYNC	VIP_VSYNC	-	-	GPIO4[16]	PWR_PROG[18]
X_VIP_HSYNC	VIP_HSYNC	-	-	GPIO4[17]	PWR_PROG[19]
X_VIP_PXCLK	VIP_PXCLK	-	-	GPIO4[18]	PWR_PROG[20]
X_CPH_CLK	CPH_CLK	-	-	GPIO2[3]	PWR_PROG[83]
X_CPH_FS_CLK	CPH_FS_CLK	-	-	GPIO2[4]	PWR_PROG[84]
X_GPIO[8]	WARM_RST_B	-	-	GPIO0[8]	PWR_PROG[31]
X_GPIO[9]	-	TMS	EF_CS_B	GPIO0[9]	PWR_PROG[32]
X_GPIO[10]	-	TDI	EF_DIN	GPIO0[10]	PWR_PROG[33]
X_GPIO[11]	-	TDO	EF_DOUT	GPIO0[11]	PWR_PROG[34]

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_GPIO[12]	-	NSRST	-	GPIO0[12]	PWR_PROG[35]
X_GPIO[13]	-	RTCK	EF_PGM	GPIO0[13]	PWR_PROG[36]
X_GPIO[14]	-	NTRST	-	GPIO0[14]	PWR_PROG[37]
X_GPIO[15]	-	TCK	EF_SCLK	GPIO0[15]	PWR_PROG[38]
X_SDA_0	SDA_0	-	-	GPIO3[18]	PWR_PROG[0]
X_SCL_0	SCL_0	-	-	GPIO3[19]	PWR_PROG[1]
X_XP	-	-	-	-	-
X_XN	-	-	-	-	-
X_YP	-	-	-	-	-
X_YN	-	-	-	-	-
VREF_ADC	-	-	-	-	-
X_AUX0	-	-	-	-	-
X_AUX1	-	-	-	-	-
X_AUX2	-	-	-	-	-
X_MCKE	MCKE	-	-	-	FIX
X_MCS_B	MCS_B	-	-	-	PWR_FIX[0]
X_MWE_B	MWE_B	-	-	-	PWR_FIX[1]
X_MRAS_B	MRAS_B	-	-	-	PWR_FIX[2]
X_MCAS_B	MCAS_B	-	-	-	PWR_FIX[3]
X_MD[31]	MD[31]	-	-	-	FIX
X_MD[30]	MD[30]	-	-	-	FIX
X_MD[29]	MD[29]	-	-	-	FIX
X_MD[28]	MD[28]	-	-	-	FIX
X_MDQM[3]	MDQM[3]	-	-	-	FIX
X_MDQS[3]	MDQS[3]	-	-	-	FIX
X_MD[27]	MD[27]	-	-	-	FIX
X_MD[26]	MD[26]	-	-	-	FIX

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_MD[25]	MD[25]	-	-	-	FIX
X_MD[24]	MD[24]	-	-	-	FIX
X_MD[23]	MD[23]	-	-	-	FIX
X_MD[22]	MD[22]	-	-	-	FIX
X_MD[21]	MD[21]	-	-	-	FIX
X_MD[20]	MD[20]	-	-	-	FIX
X_MDQM[2]	MDQM[2]	-	-	-	FIX
X_MDQS[2]	MDQS[2]	-	-	-	FIX
X_MD[19]	MD[19]	-	-	-	FIX
X_MD[18]	MD[18]	-	-	-	FIX
X_MD[17]	MD[17]	-	-	-	FIX
X_MD[16]	MD[16]	-	-	-	FIX
X_MD[15]	MD[15]	-	-	-	FIX
X_MD[14]	MD[14]	-	-	-	FIX
X_MD[13]	MD[13]	-	-	-	FIX
X_MD[12]	MD[12]	-	-	-	FIX
X_MDQM[1]	MDQM[1]	-	-	-	FIX
X_MDQS[1]	MDQS[1]	-	-	-	FIX
X_MD[11]	MD[11]	-	-	-	FIX
X_MD[10]	MD[10]	-	-	-	FIX
X_MD[9]	MD[9]	-	-	-	FIX
X_MD[8]	MD[8]	-	-	-	FIX
X_MD[7]	MD[7]	-	-	-	FIX
X_MD[6]	MD[6]	-	-	-	FIX
X_MD[5]	MD[5]	-	-	-	FIX
X_MD[4]	MD[4]	-	-	-	FIX
X_MDQM[0]	MDQM[0]	-	-	-	FIX
X_MDQS[0]	MDQS[0]	-	-	-	FIX

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_MD[3]	MD[3]	-	-	-	FIX
X_MD[2]	MD[2]	-	-	-	FIX
X_MD[1]	MD[1]	-	-	-	FIX
X_MD[0]	MD[0]	-	-	-	FIX
X_MCLK_O	MCLK	-	-	-	PWR_PROG[116]
X_MCLKB_O	-	-	-	-	-
X_M_BA[1]	M_BA[1]	-	-	-	FIX
X_M_BA[0]	M_BA[0]	-	-	-	FIX
X_MA[12]	MA[12]	-	-	-	FIX
X_MA[11]	MA[11]	-	-	-	FIX
X_MA[10]	MA[10]	-	-	-	FIX
X_MA[9]	MA[9]	-	-	-	FIX
X_MA[8]	MA[8]	-	-	-	FIX
X_MA[7]	MA[7]	-	-	-	FIX
X_MA[6]	MA[6]	-	-	-	FIX
X_MA[5]	MA[5]	-	-	-	FIX
X_MA[4]	MA[4]	-	-	-	FIX
X_MA[3]	MA[3]	-	-	-	FIX
X_MA[2]	MA[2]	-	-	-	FIX
X_MA[1]	MA[1]	-	-	-	FIX
X_MA[0]	MA[0]	-	-	-	FIX
X_DF_AD[7]	DF_AD[7]	SD_DAT_0[7]	SD_DAT_2[7]	-	PWR_PROG[110]
X_DF_AD[6]	DF_AD[6]	SD_DAT_0[6]	SD_DAT_2[6]	-	PWR_PROG[147]
X_DF_AD[5]	DF_AD[5]	SD_DAT_0[5]	SD_DAT_2[5]	-	PWR_PROG[148]
X_DF_AD[4]	DF_AD[4]	SD_DAT_0[4]	SD_DAT_2[4]	-	PWR_PROG[149]
X_DF_AD[3]	DF_AD[3]	SD_DAT_0[3]	SD_DAT_2[3]	-	PWR_PROG[150]

Pin Name	Function 1	Function 2	Function 3	GPIO	Sleep Status Control
X_DF_AD[2]	DF_AD[2]	SD_DAT_0[2]	SD_DAT_2[2]	-	PWR_PROG[151]
X_DF_AD[1]	DF_AD[1]	SD_DAT_0[1]	SD_DAT_2[1]	-	PWR_PROG[152]
X_DF_AD[0]	DF_AD[0]	SD_DAT_0[0]	SD_DAT_2[0]	-	PWR_PROG[153]
X_DF_CLE	DF_CLE	SD_CLK_0	-	-	PWR_PROG[132]
X_DF_ALE	DF_ALE	SD_CMD_0	-	-	PWR_PROG[133]
X_DF_WE_B	DF_WE_B	SD_CLK_2	-	-	PWR_PROG[120]

Table 2: SiRFatlasIV Pin Share

Power List	
VDD_PDN	1.2V, core power. When SoC entering sleep mode, it is shut down by X_PWR_EN.
VDD_PRE	1.2V, core power. To be kept on when SoC entering sleep mode to maintain the fundamental digital logic.
VDDIO_N	3.3V, I/O power (will be updated according to ATE results).
VDDIO_L	3.3V, I/O power (will be updated according to ATE results).
VDDIO	3.3V, I/O power.
VDDIO_MEM	2.5V or 2.6V for normal DDR SDRAM, 1.8V for mobile DDR SDRAM. Memory I/O power.
VREF_MEM	1.25V or 1.3V. Half voltage of VDDIO_MEM, when VDDIO_MEM is 2.5V or 2.6V for SSTL pad type of DDR SDRAM.
VDD_PLL	1.2V, digital power for internal PLL.
VDDIO_PLL	3.3V, I/O power for internal PLL.
VDDA_PLL2	1.2V, analog power for internal PLL.
VDDA_PLL1	1.2V, analog power for internal PLL.
VDD_RTC	1.2V, digital power for RTC.
VDD_LVR	1.62~3.63V, power input for internal LVR, which can provide output power 1.2V for VDD_RTC.
VDDIO_RTC	3.3V, I/O power for RTC.
VDDA2V5_USB	2.5V, analog power for USB.
VDDA3V3_USB	3.3V, analog power for USB.

VDD_TSC	1.2V, digital power for internal touch screen controller.
VDDIO_TSC	VDDIO_TSC: 2.5V, I/O power for touch screen controller. **NOTE** — The value of power supply on the VDDIO_TSC must equal to the value on VDDA_TSC. VDDIO_TSC must be connected to the VDDA_TSC on the board.
VDDA_TSC	2.5V, analog power for touch screen controller.
VREF_ADC	2.0V~VDDA_TSC, reference voltage for the ADC built in SoC when doing auxiliary measurement. When doing auxiliary measurement, it can be directly connected to VDDA_TSC or other power supply within its valid range (2.0V~VDDA_TSC), or it can be left disconnected if the internal reference voltage is used by the TS Controller register configuration.
VPROG	2.5V, programming power for the internal eFuse.
Ground List	
VSS	The main digital ground domain.
VSSIO_RTC	I/O ground for RTC. It is connected to VSS domain directly.
VSS_RTC	Digital ground for RTC. It is connected to VSS domain directly.
VSSA_PLL1	Analog ground for PLL. It and VSSA_PLL2 belong to independent analog ground domain, which is connected to VSS domain by bead or resistor.
VSSA_PLL2	Analog ground for PLL. It and VSSA_PLL1 belongs to independent analog ground domain, which is connected to VSS domain by bead or resistor.
VSS_PLL	Digital ground for PLL. It is connected to VSS domain directly.
VSSIO_PLL	I/O ground for PLL. It is connected to VSS domain directly.
VSSA_TSC	Analog ground for the Touch Screen Controller.
VSSA_USB	Analog ground for USB.

Table 3: SiRFatlasIV Power/Ground List

Ball Location	Ball Name	Ball Location	Ball Name	Ball Location	Ball Name
A1	X_L_PCLK	G1	X_GPS_SGN	N17	X_XP
A2	X_L_LCK	G2	X_GPS_SAMPLE_CLK	N18	X_XN
A3	X_DF_CS_B[0]	G3	X_LDD[14]	P1	X_AC97_BIT_CLK
A4	X_DF_WE_B	G4	X_LDD[15]	P2	X_AC97_DIN
A5	X_DF_CLE	G5	VDD_PRE	P3	X_AC97_SYNC
A6	X_DF_AD[3]	G8	VSS	P4	X_RXD_1
A7	X_MA[0]	G9	VSS	P5	VDDIO
A8	X_MA[3]	G10	VSS	P6	VDDIO
A9	X_MA[12]	G11	VSS	P7	VDD_PRE
A10	X_MA[9]	G14	VDDIO_MEM	P8	VDD_PDN
A11	X_MCLK_O	G15	X_MDQS[3]	P9	VDD_PDN
A12	X_MD[6]	G16	X_MD[26]	P10	VDD_PDN
A13	X_MD[7]	G17	X_MD[25]	P11	VDDIO
A14	X_MD[8]	G18	X_MD[29]	P12	VDDIO
A15	X_MD[11]	H1	X_GPS_CLK	P13	VDDIO
A16	X_MD[13]	H2	X_GPS_MAG	P14	VDD_PDN
A17	VSS	H3	X_GPIO[2]	P15	X_GPIO[14]
A18	VREF_MEM	H4	X_GPIO[1]	P16	X_GPIO[13]
B1	X_L_FCK	H5	VDDIO_L	P17	X_GPIO[12]
B2	X_L_DE	H7	VSS	P18	X_GPIO[11]
B3	X_DF_CS_B[1]	H8	VSS	R1	X_TXD_0
B4	X_DF_RY_BY	H9	VSS	R2	X_RXD_0
B5	X_DF_ALE	H10	VSS	R3	X_TXD_1
B6	X_DF_AD[5]	H11	VSS	R4	X_PWR_EN
B7	X_MA[2]	H12	VSS	R5	X_USB_VBUS
B8	X_MA[1]	H14	VDDIO_MEM	R6	X_USB_TEST_GPANAIO
B9	X_MA[8]	H15	X_MDQM[3]	R7	VDDIO_PLL
B10	X_MA[6]	H16	X_MD[31]	R8	VSSIO_PLL
B11	X_MCLKB_O	H17	X_MD[30]	R9	X_TEST_MODE[5]
B12	X_MD[0]	H18	X_MCS_B	R10	X_TEST_MODE[4]

Ball Location	Ball Name	Ball Location	Ball Name	Ball Location	Ball Name
B13	X_MDQS[0]	J1	X_SD_CD_B_1	R11	X_TEST_MODE[2]
B14	X_MD[10]	J2	X_GPIO[3]	R12	X_TEST_MODE[0]
B15	X_MD[12]	J3	X_GPIO[0]	R13	X_SCAN_EN
B16	X_MDQM[1]	J4	VPROG	R14	X_VIP_PXD[9]
B17	X_MD[16]	J5	VDDIO	R15	X_GPIO[10]
B18	X_MD[17]	J7	VSS	R16	X_GPIO[9]
C1	X_LDD[2]	J8	VSS	R17	X_GPIO[8]
C2	X_LDD[0]	J9	VSS	R18	X_CPH_FS_CLK
C3	X_LDD[1]	J10	VSS	T1	X_UTXD_0
C4	X_DF_RE_B	J11	VSS	T2	X_URXD_1
C5	X_DF_AD[1]	J12	VSS	T3	X_UTFS_1
C6	X_DF_AD[4]	J14	VDDIO_MEM	T4	X_URFS_1
C7	X_DF_AD[7]	J15	X_MCKE	T5	X_USB_ID
C8	X_MA[5]	J16	X_MRAS_B	T6	VSSA_USB
C9	X_MA[4]	J17	X_MCAS_B	T7	VSS_PLL
C10	X_M_BA[0]	J18	X_MWE_B	T8	VSSA_PLL2
C11	X_M_BA[1]	K1	X_SD_CLK_1	T9	X_RESET_B
C12	X_MD[2]	K2	X_SD_CMD_1	T10	X_TEST_MODE[3]
C13	X_MD[3]	K3	X_SD_VCC_ON_1	T11	X_TEST_MODE[1]
C14	X_MDQM[0]	K4	X_SD_WP_B_1	T12	VDD_LVR
C15	X_MD[9]	K5	VDDIO	T13	X_ ALARM_WAKEUP
C16	X_MD[14]	K7	VSS	T14	X_VIP_PXD[8]
C17	X_MD[19]	K8	VSS	T15	X_VIP_PXD[5]
C18	X_MD[18]	K9	VSS	T16	X_VIP_PXD[2]
D1	X_LDD[3]	K10	VSS	T17	X_VIP_PXD[0]
D2	X_LDD[4]	K11	VSS	T18	X_CPH_CLK
D3	X_LDD[7]	K12	VSS	U1	X_URXD_0
D4	X_DF_WP_B	K14	VDDIO_MEM	U2	X_UTFS_0
D5	X_DF_AD[0]	K15	VDD_PRE	U3	X_UTXD_1
D6	X_DF_AD[2]	K16	X_GPIO[15]	U4	X_USB_DN
D7	X_DF_AD[6]	K17	X_SDA_0	U5	VDDA2V5_USB

Ball Location	Ball Name	Ball Location	Ball Name	Ball Location	Ball Name
D8	X_MA[7]	K18	X_SCL_0	U6	X_USB_RREFEXT
D9	X_MA[10]	L1	X_SD_DAT_1[1]	U7	VDD_PLL
D10	X_MA[11]	L2	X_SD_DAT_1[0]	U8	VDDA_PLL2
D11	VDD_PRE	L3	X_SD_DAT_1[2]	U9	X_CKO_0
D12	X_MD[4]	L4	X_SD_DAT_1[3]	U10	VSS_RTC
D13	X_MD[5]	L5	VDDIO	U11	VSSIO_RTC
D14	X_MD[1]	L7	VSS	U12	X_XIN
D15	X_MDQS[1]	L8	VSS	U13	X_GPIO[4]
D16	X_MD[15]	L9	VSS	U14	X_GPIO[6]
D17	X_MD[21]	L10	VSS	U15	X_VIP_PXD[7]
D18	X_MD[20]	L11	VSS	U16	X_VIP_PXD[4]
E1	X_LDD[5]	L12	VSS	U17	X_VIP_PXD[1]
E2	X_LDD[6]	L14	VDD_PDN	U18	X_VIP_VSYNC
E3	X_LDD[10]	L15	VDD_TSC	V1	X_USCLK_0
E4	X_LDD[11]	L16	X_AUX0	V2	X_URFS_0
E5	VDDIO_N	L17	X_YP	V3	X_USCLK_1
E6	VDDIO_N	L18	X_YN	V4	X_USB_DP
E7	VDD_PDN	M1	X_SD_CLK_3	V5	VDDA3V3_USB
E8	VDD_PDN	M2	X_SD_CMD_3	V6	VSSA_PLL1
E9	VDD_PDN	M3	X_SD_DAT_3[0]	V7	VDDA_PLL1
E10	VDDIO_MEM	M4	X_SD_DAT_3[1]	V8	X_XINW
E11	VDDIO_MEM	M5	VDDIO	V9	X_XOUTW
E12	VDDIO_MEM	M8	VSS	V10	VDD_RTC
E13	VDDIO_MEM	M9	VSS	V11	VDDIO_RTC
E14	VDDIO_MEM	M10	VSS	V12	X_XOUT
E15	VDD_PRE	M11	VSS	V13	X_GPIO[7]
E16	X_MD[22]	M14	VDD_PDN	V14	X_GPIO[5]
E17	X_MD[23]	M15	X_AUX2	V15	X_VIP_PXD[6]
E18	X_MDQS[2]	M16	VSSA_TSC	V16	X_VIP_PXD[3]
F1	X_LDD[8]	M17	VREF_ADC	V17	X_VIP_HSYNC
F2	X_LDD[9]	M18	VDDA_TSC	V18	X_VIP_PXCLK

Ball Location	Ball Name	Ball Location	Ball Name	Ball Location	Ball Name
F3	X_LDD[12]	N1	X_CKO_1	-	-
F4	X_LDD[13]	N2	X_SD_DAT_3[2]	-	-
F5	VDDIO_L	N3	X_SD_DAT_3[3]	-	-
F14	VDDIO_MEM	N4	X_AC97_DOUT	-	-
F15	X_MD[27]	N5	VDDIO	-	-
F16	X_MDQM[2]	N14	VDD_PDN	-	-
F17	X_MD[28]	N15	VDDIO_TSC	-	-
F18	X_MD[24]	N16	X_AUX1	-	-

Table 4: SiRFatlasIV Ball Assignment

Pad Type Description

Name	Direction	Output	Input	Driving (mA)
PDBxDGZ	I/O	CMOS tri-state	Normal	x
PDBxSDGZ	I/O	CMOS tri-state	Schmitt	x
PDDxDGZ	I/O	CMOS tri-state	Pull-down	x
PDDxSDGZ	I/O	CMOS tri-state	Schmitt + pull-down	x
PDDDGZ	I	-	Pull-down	-
PDDWxDGZ	I/O	CMOS tri-state	Program pull-down	x
PDISDGZ	I	-	Schmitt	-
PDIDGZ	I	-	Normal	-
PDOxCDG	O	CMOS	-	x
PDTxDGZ	O	CMOS tri-state	-	x
PDUxSDGZ	I/O	CMOS tri-state	Schmitt + pull-up	x
PDUSDGZ	I	-	Schmitt + pull-up	x
PDUWxDGZ	I/O	CMOS tri-state	Program pull-up	x
PDXO01M_GUC_65LP	32 KHz crystal using pad			
PDXOE3DG	12 MHz crystal using pad			
PMEMIO	Program memory I/O pad			
PMEMIODIFF	Program memory clock pad			
PDB3A	Analog pad			
PDBANA_5VT	Analog pad			

Table 5: SiRFatlasIV Pad Type Description

NOTE – The letter x in Pad Name in the above table is a number representing the driving current.

ELECTRICAL AND TIMING CHARACTERISTICS

Absolute Maximum Ratings

Parameter		Min.	Max.
VDDA_PLL1 VDDA_PLL2	PLL analog power (V)	-0.3	1.4
VDD_PLL	PLL digital power (V)	-0.3	1.4
VDDIO_PLL	Main crystal pad power (V)	-0.3	4.0
VDDIO_RTC	RTC crystal pad power (V)	-0.3	4.0
VDD_LVR	LVR analog power (V)	-0.3	4.0
VDD_PDN VDD_PRE	Main core power (V)	-0.3	1.4
VDDIO	I/O pads power except memory interface (V)	-0.3	4.0
VDDIO_MEM	Memory interface power (V)	-0.3	4.0
VREF_MEM	Memory interface Vref, only needed when connecting normal DDR (V)	-0.3	2.0
VDD_TSC	TSC digital power (V)	-0.3	1.4
VDDA_TSC	TSC analog power (V)	-0.3	4.0
VDDIO_TSC	VDDIO_TSC: TSC analog IO power; VDDIO_TSC must be connected to the VDDA_TSC on the board.	-0.3	4.0
VREF_ADC	TSC reference power (V)	-0.3	4.0
VDDA3V3_USB	USB analog power (V)	-0.3	4.0
VDDA2V5_USB	USB analog power (V)	-0.3	4.0
VPROG	EFUSE power (V)	-0.3	4.0
Vinos	Input voltage overshoot (V)	-	0.5
Vinus	Input voltage undershoot (V)	-	0.5
Ts	Storage ambient temperature (°C)	-65	125

Table 6: Absolute Maximum Ratings

NOTE – Absolute maximum ratings are stress ratings only, functional operations tested to the maximum stress capacity are not guaranteed. Stresses beyond those listed in the table above may affect device reliability and cause permanent damage.

Recommended Operating Conditions

Parameter		Min.	Typical	Max.	Comments
VDDA_PLL1 VDDA_PLL2	PLL analog power (V)	1.14	1.20	1.26	-
VDD_PLL	PLL digital power (V)	1.14	1.20	1.26	-
VDDIO_PLL	Main crystal pad power (V)	3.0	3.3	3.6	-
VDDIO_RTC	RTC crystal pad power (V)	2.3	3.3	3.6	-
VDD_LVR	LVR analog power (V)	2.3	3.3	3.6	
VDD_PDN VDD_PRE	Main core power (V)	1.25	1.3	1.35	-
VDDIO	I/O pads power except memory interface (V)	3.0	3.3	3.6	-
VDDIO_MEM	Memory interface power (V)	2.5	2.6	2.7	When connecting DDR SDRAM
			TBD		When connecting MDDR SDRAM
VREF_MEM	Memory interface Vref, only needed when connecting normal DDR (V)	0.49 x VDDIO_MEM	0.5 x VDDIO_MEM	0.51 x VDDIO_MEM	For SSTL, VDDIO_MEM/2, only necessary in normal DDR mode
VDD_TSC	TSC digital power (V)	1.14	1.20	1.26	-
VDDA_TSC	TSC analog power (V)	2.25	2.5	2.75	-
VDDIO_TSC	TSC digital power (V)	-	-	-	- VDDIO_TSC: TSC analog IO power; VDDIO_TSC must be connected to the VDDA_TSC on the board.
VREF_ADC	TSC reference power (V)	2.0	VDDA_TSC	VDDA_TSC	-
VDDA3V3_USB	USB analog power (V)	3.0	3.3	3.6	-
VDDA2V5_USB	USB analog power (V)	2.25	2.5	2.75	-
VPROG	EFUSE power (V)	2.25	2.5	2.75	When programing the eFuse, apply this voltage on VPROG.In reading or other modes, make sure it

Parameter		Min.	Typical	Max.	Comments
					connects with GND.
Vinos	Input voltage overshoot (V)	-	0	0.3	-
Vinus	Input voltage undershoot (V)	-	0	0.3	-
To	Operation ambient temperature (˚C)	-20	25	70	Industry grade is TBD
Tj	Internal transistor junction temperature (˚C)	-20	25	125	-

Table 7: Recommended Operating Conditions

NOTE – The conditions in the table above are tested and recommended (unless specified as “to be qualified”). Any device operations not listed in this table may not be guaranteed.

Power-On and Power-Off Sequences

There are no requirements for the power-off sequence. Customers can decide which voltage is to be turned off based on their application needs.

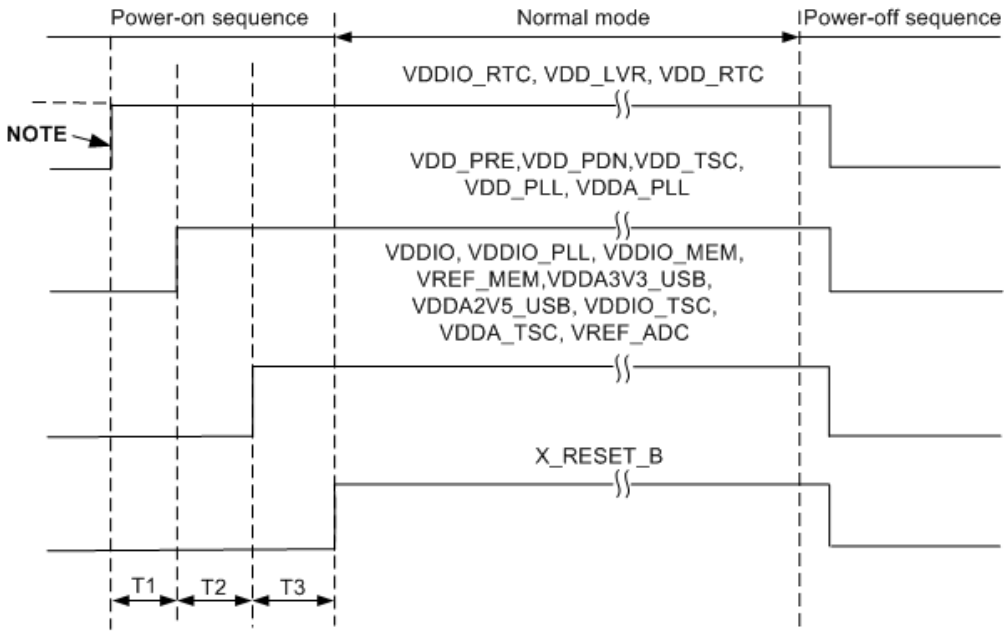
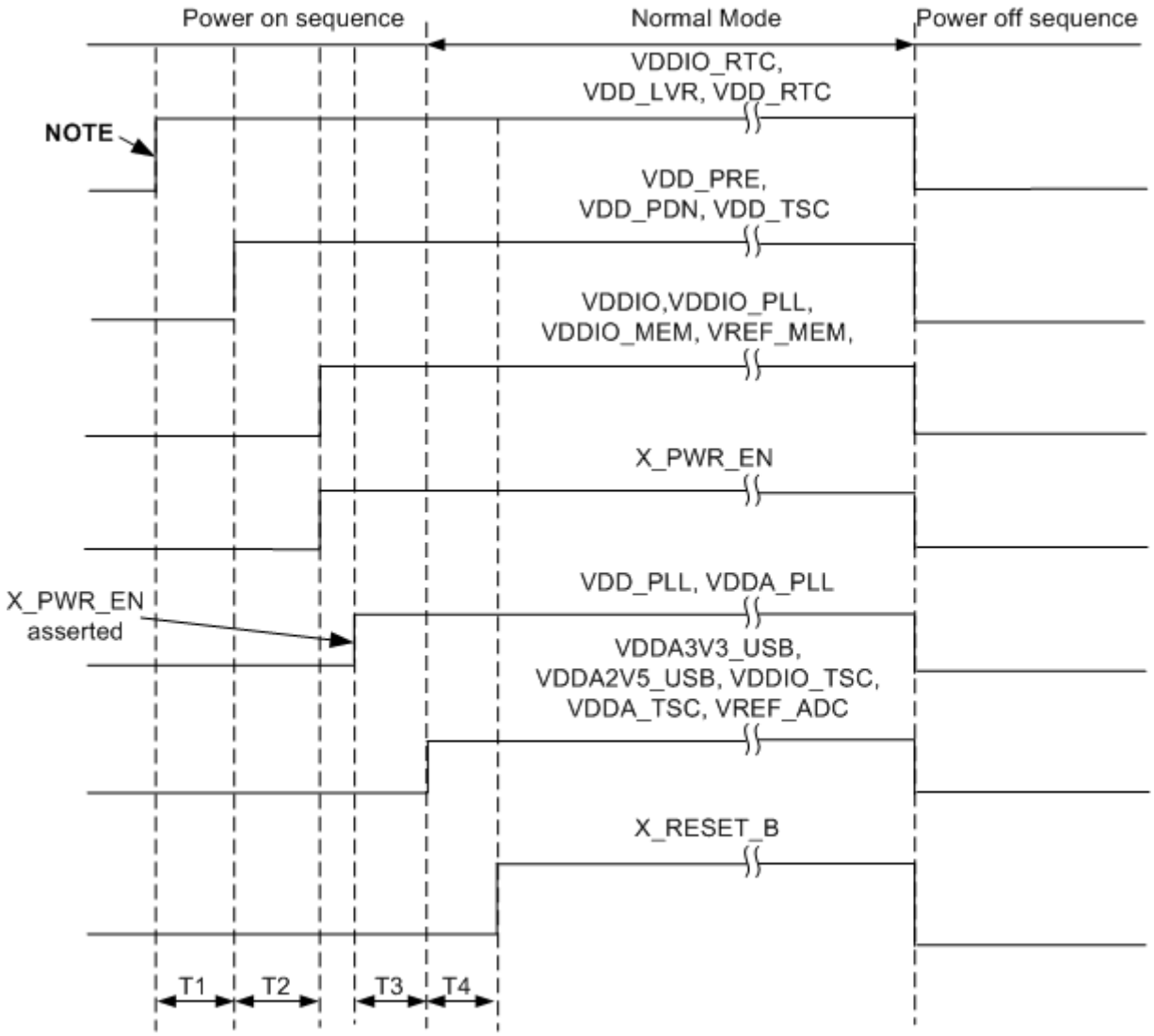


Figure 6: Power On/Off Sequence (1)

In Figure 6,

- 2ms ⩾ T2 ⩾ 0 ms
- T3 ⩾ 2 ms



NOTE – RTCIO_RTC, VDD_LVR, and VDD_RTC are always on or T1≥ 1ms.

Figure 7: Power On/Off Sequence (2)

In Figure 7:

- T2 ⩾ 0 ms
- 2 ms ⩾ T3 ⩾ 0 ms
- T4 ⩾ 2 ms

Deep Sleep and Wakeup Sequences

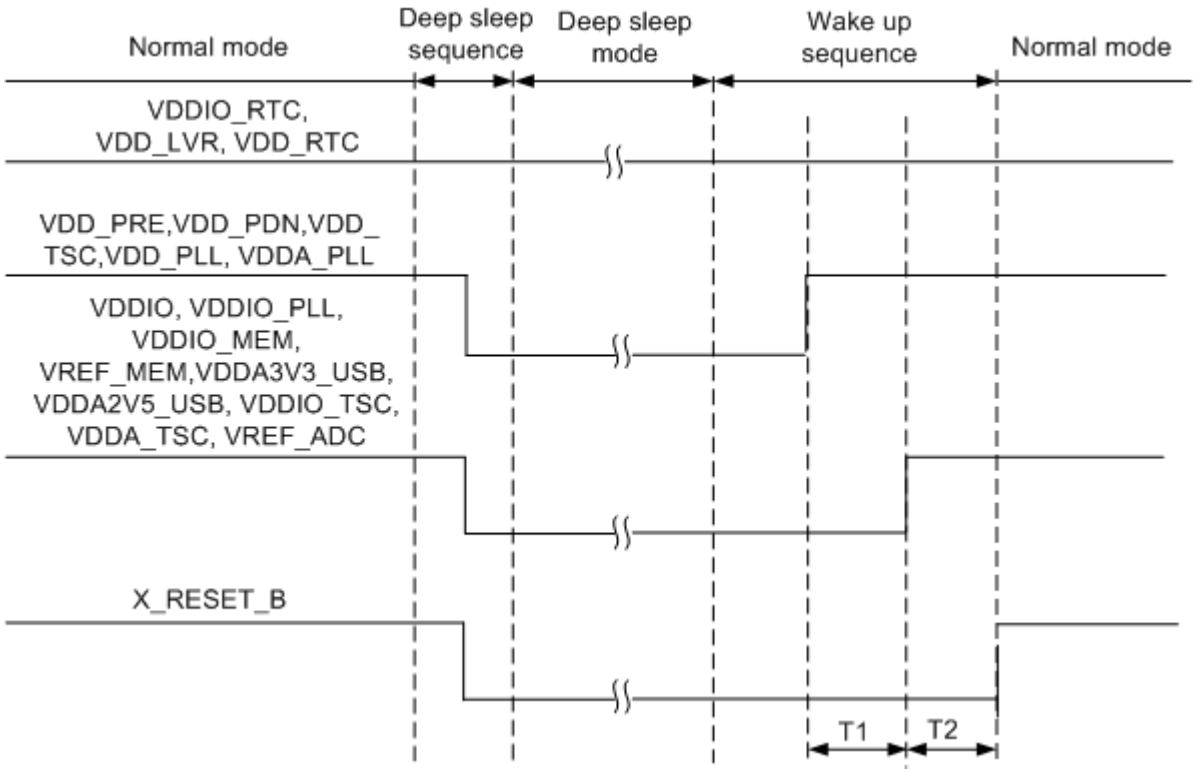


Figure 8: Deep Sleep Wakeup Sequence

In Figure 8:

- 2 ms ⩾ T1 ⩾ 0 ms
- T2 ⩾ 2ms

Sleep and Wakeup Sequences

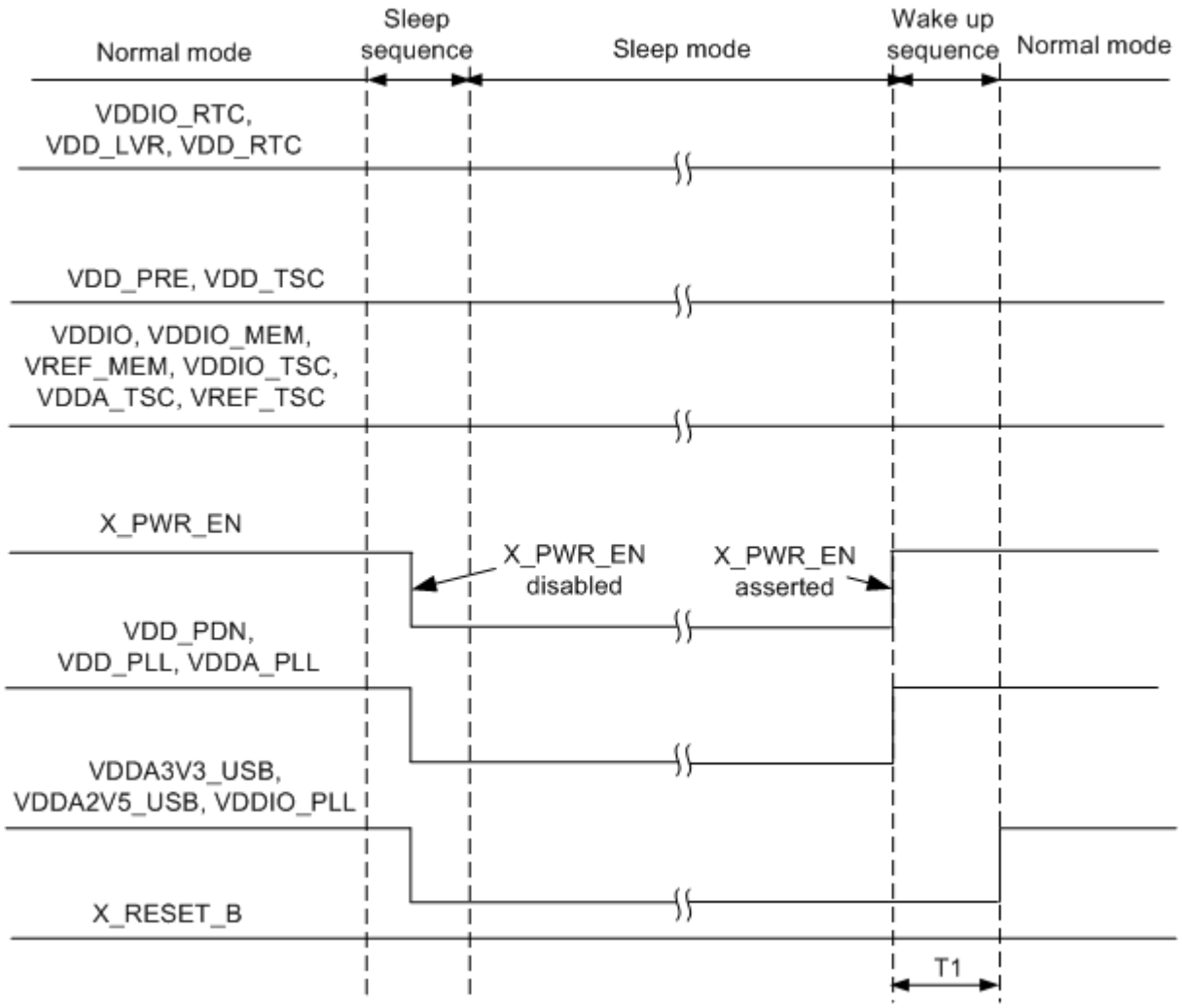


Figure 9: Sleep Wakeup Sequence

In Figure 9:

- 2 ms ⩾ T1 ⩾ 0 ms
- X_RESET_B is always high.

Thermal Characteristics

Major thermal dissipation paths can be illustrated as follows:

- T_J: the maximum junction temperature
- T_A: the ambient or environment temperature
- T_C: the maximum compound surface temperature
- T_B: the maximum surface temperature of PCB bottom
- P: total input power

The thermal parameter can be defined as the following:

1. Junction to ambient thermal resistance:

$$\Theta_{JA} = \frac{T_J - T_A}{P} \qquad (1)$$

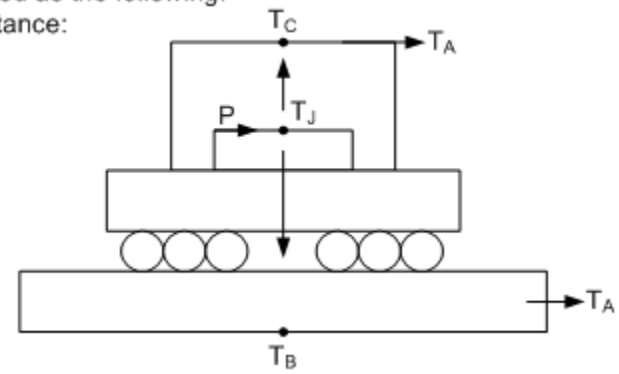
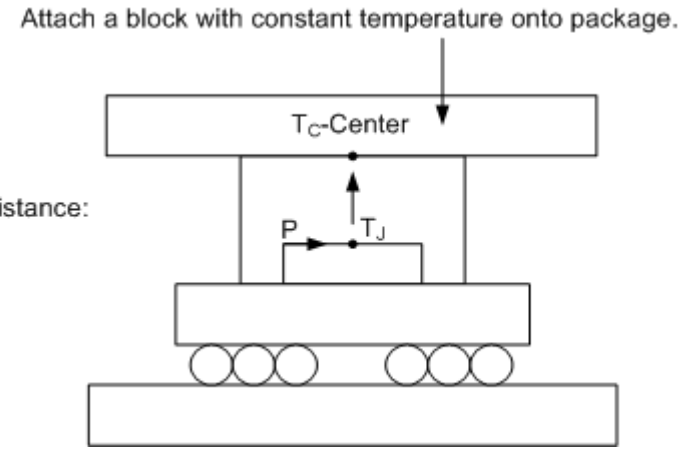


Figure 10: Junction to Ambient Thermal Resistance



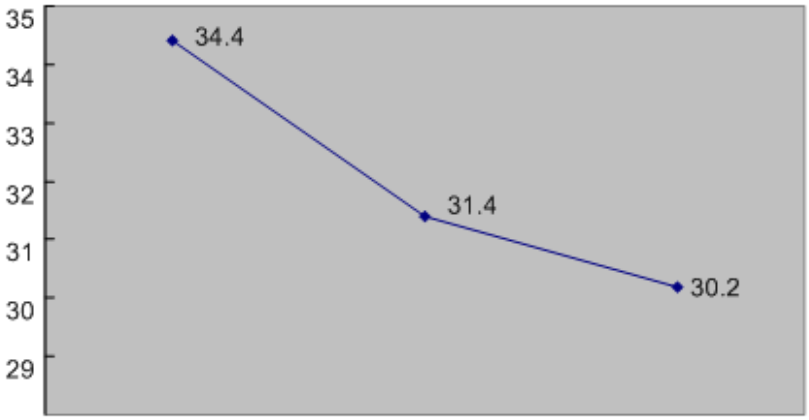
2. Junction to case thermal resistance:

$$\Theta_{JC} = \frac{T_J - T_C}{P} \qquad (2)$$

Figure 11: Junction to Case Thermal Resistance

Thermal Performance

The junction-to-ambient thermal resistance is utilized to evaluate thermal performance for this package and to predict the power dissipation capability by giving ambient and maximum junction temperatures.



θJA (°C/W)	34.4	31.4	30.2
Air Flow (m/s)	0	1	2

Figure 12: Thermal Performance of SiRFatlasⅣ under Forced Convection

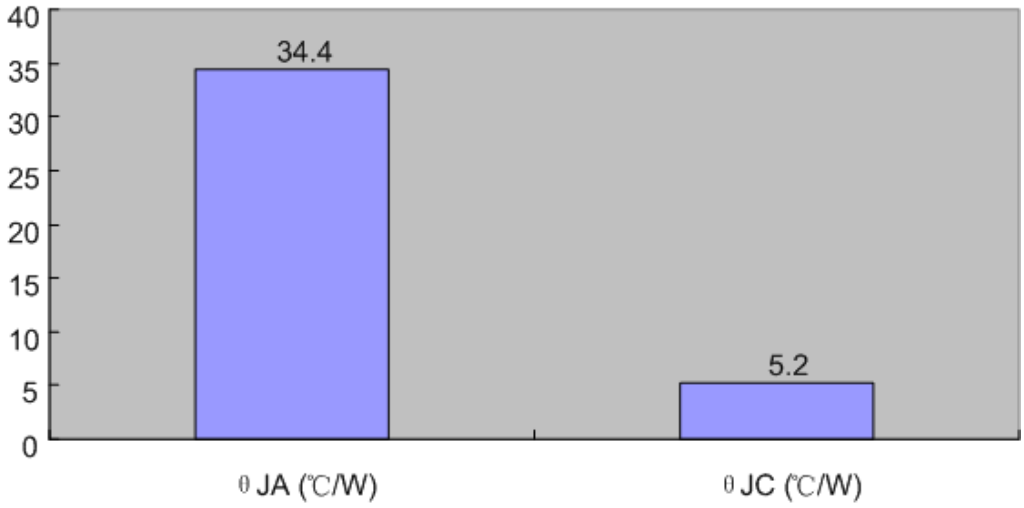


Figure 13: Thermal Performance of TFBGA under Natural Convection

Reliability Test Specifications

The reliability test specifications of SiRFatlasIV follow the JEDEC testing standard as part of product qualification plan. Detailed testing items and conditions are listed in the table below.

Test Item	Test Method	Test Condition	Number of Lots Sample Lot/Size	Criteria
ESD-HBM	JEDEC 22-A114-A	Human Body Model (HBM): R=1.5kΩ/C=100pF	1/6	HBM≥+/-2KV
ESD-CDM	JEDEC 22-C101	Charge Device Model (CDM): +/-400V	1/6	CDM≥+/-400V
ESD-MM	JEDEC 22-A115	MM (Machine Model): R=0kΩ/C=200	1/6	MM≥+/-150V
Latch up	JEDEC 78	+(Inom+100mA)/-100mA /1.5X max. Vsupply, Max. OP AMB. Temp	1/6	1.4x Imon
HTOL	JESD22-A108	125°C/ 1.1*VCC /1000hrs Read point: 168 hours, 500 hours, 1000 hours	2/77	LTPD=5% (Acc/Rej=0/1)
NBTI	JEDEC 22-A108	125°C/1.4*Vcc (depending on Tj@pretest)/1000hrs Read point: 168 hours, 500 hours, 1000 hours.	1/77	LTPD=5% (Acc/Rej=0/1)
Pre-conditioning	JESD 22-A113, JEDEC J-STD-020	SAT, -65/150oC, 5 cycle, bake@30C/60%RH 192 hours IR*3, visual/func./SAT. 2. Peak 260oC IR Reflow for Pb-free	3/150	0/1
TCT	JEDEC 22-A104	-65°C~+150°C/1000 cycles/Pre-condition Read point: 500 cycles, 1000 cycles	3/45	LTPD=5% (Acc/Rej=0/1)
Bias HAST	JESD-A110	1.1*Vcc/130°C/85%RH 96 hours Pre-condition	3/45	LTPD=5% (Acc/Rej=0/1)
HTST	JESD22A-103-A	150°C/1000 hours, no bias Read point: 500hrs, 1000hrs.	3/45	LTPD=5% (Acc/Rej=0/1)
PCT	JESD22-A102B	121°C/100%RH, 15 PSI 96 hours	1/45	Reference only

Table 8: Reliability Qualification Summary

IR Reflow Profile

- Recommended reflow profile:
  - Peak-temp is 20°C-30°C above 217°C.
  - Soaking at 140°C - 160°C about 60 - 90 seconds
  - Temperature maintained above 217°C: 40 - 60 seconds
  - Ramp with 1-2°C/sec to 140-160°C
  - Rate of rise from 160°C to 217°C is 2-3°C/sec
-

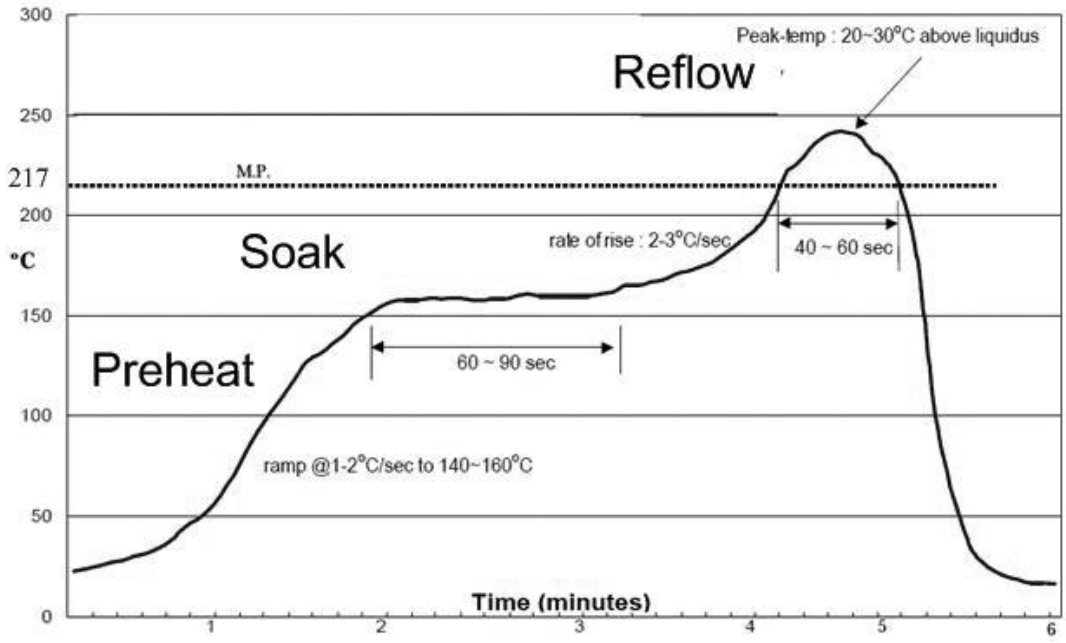


Figure 14: IR-Reflow Profile

DC Electrical Specifications

Normal Pad I/O DC Characteristics

Parameter			Min.	Typical	Max.	Comments
V_{IL}	Input low voltage (V)		-0.3	-	0.8	VDD_IO pads
V_{IH}	Input high voltage (V)		2.0	-	3.6	VDD_IO pads
V_{OL}	Output low voltage (V)		-	-	0.4	VDD_IO pads
V_{OH}	Output high voltage (V)		2.4	-	-	VDD_IO pads
V_{T+}	Schmitt trig. low to high threshold point (V)		1.56	1.68	1.77	Schmitt trig pad: PDBxSDGZ, PDDxSDGZ, PDUxSDGZ, PDUSDGZ
V_{T-}	Schmitt trig. High to low threshold point (V)		1.15	1.23	1.31	Schmitt Trig pad: PDBxSDGZ, PDDxSDGZ, PDUxSDGZ, PDUSDGZ
I-in	Input leakage current @VI=3.3V or 0V (µA)		-	-	±10	-
I_{OZ}	Tri-state output leakage current @VO=3.3V or 0V (µA)		-	-	±10	-0
R_{PD}	Internal equivalent pull-up resistor (KΩ)		34	-	82	For these pads: PDDxDGZ, PDDxSDGZ, PDDDGZ, PDDWxDGZ
R_{PU}	Internal equivalent pull-down resistor (KΩ)		26	-	60	For these pads: PDUxDGZ, PDUxSDGZ, PDUDGZ, PDUWxDGZ
Vpu	GPIO Pull up power voltage(V)		2.5	2.6	2.7	VDD_IO set to 3.3V
I_{OL}	Low level output current @V_{OL} (max.) (mA)	4 mA	4	-	-	4mA pad: PDB04SDGZ, PDD04DGZ, PDD04SDGZ, PDDW04DGZ, PDO04CDG, PDT04DGZ, PDU04SDGZ, PDUW04DGZ 8mA pad: PDB08SDGZ, PDD08SDGZ,
		8 mA	8	-	-	
		16 mA	16	-	-	
I_{OH}	High level output Current @V_{OH}=(min.)	4 mA	4	-	-	
		8 mA	8	-	-	
		16m	16	-	-	

Parameter			Min.	Typical	Max.	Comments
	(mA)	A				PDDW08DGZ, PDO08CDG, PDT08DGZ, PDUW08DGZ 16mA pad: PDO16CDG, PDUW16DGZ

Table 9: Normal Pad I/O DC Characteristics

Memory Pad I/O DC Characteristics

Parameter		Min.	Typical	Max.	Comments
V_{IL}	Input low voltage (V)	-0.3	-	Vref - 0.15	Memory pads in DDR/SSTL2 mode
		-0.3	-	Vref - 0.125	Memory pads in SSTL18 mode
		-0.3	-	0.36	Memory pads in mDDR mode
V_{IH}	Input high voltage (V)	Vref + 0.15	-	VDDIO_MEM + 0.3	Memory pads in DDR/SSTL2 mode
		Vref + 0.125	-	VDDIO_MEM + 0.3	Memory pads in SSTL18 mode
		1.44		VDDIO_MEM + 0.3	Memory pads in mDDR mode
V_{OL}	Output low voltage (V)	-	-	0.56	Memory pads in DDR/SSTL2 mode
		-	-	0.28	Memory pads in SSTL18 mode
		-	-	0.28	Memory pads in MDDR mode
V_{OH}	Output high voltage (V)	1.74	-	-	Memory pads in DDR/SSTL2 mode
		VDDIO_MEM - 0.28	-	-	Memory pads in SSTL18 mode
		1.62	-	-	Memory pads in mDDR mode

Table 10: Memory Pad I/O DC Characteristics

LVR Electrical Characteristics

Parameter	Min.	Typical	Max.
Power Supply			
Quiescent current: (µA)	-	8	-
Temperature operation range: Ta (°C)	-20	25	70
Analog Output			
Output voltage (V)	0.86	0.96	1.06
Load current (mA)	-	-	1.0

Table 11 : LVR Electrical Characteristics

TSC and ADC Characteristics

NOTE – All values in the above table were measured at a temperature of 70°C.

Parameter		Conditions	Min.	Typical	Max.
ADC input Impendence (Ω)		Test pin is X_AUX[4:0]	500K	1M	2M
Analog Biasing					
Resistance value between ref and a gnd (KΩ)		-	-	96	-
Power supply Requirement					
Current consumption VDDA_TSC (µA)		-	-	490	-
Current consumption VDD_TSC (µA)		-	-	10	-
Power down current VDDA_TSC(µA)		-	-	8	-
Power down current VDD_TSC (µA)		-	-	2	-
Touch Screen Interface					
Switch drivers on resistance (Ω)		GND and VDD switches	-	- 10	-
Conversion Characteristics					
With external voltage reference	DNL (LSB)	fin = 1 KHz	-	-	+/-2
	INL (LSB)	fin = 1 KHz	-	-	+/-2
	Gain and Offset Error (%FS)	-	-	-	+/-2

Table 12: TSC and ADC Characteristics

Power Consumption

Power Consumption in Typical Cases

The following table lists typical power consumption details under the following testing conditions:

- ARM 500MHz, DSP 250MHz, System-bus 250MHz, I/O 125MHz, DDR (clock rate is166MHz)
- Ambient temperature: 25°C
- GPS acquisition + Mp3 decoding + MediaQ running + Mosquito running + Memory pattern test
- All powers are in typical voltage

Power Domain	Included Power Pins	Typical Power Consumption (mW)	Comments
PLL	VDDA_PLL1 VDDA_PLL2 VDD_PLL VDDIO_PLL	3 ~ 6	-
RTC	VDD_RTC VDDIO_RTC VDD_LVR	1 ~ 5	-
Core	VDD_PDN VDD_PRE	400 ~ 550	-
TSC	VDD_TSC VDDA_TSC VDDIO_TSC VREF_ADC	<1	This value depends on application. In this scenario, it is less than 1mW.
USB	VDDA3V3_USB VDDA2V5_USB	1 ~ 5	This value depends on application. It is less than 5mW in this scenario.
I/O pads	VDDIO	10 ~ 80	This value depends on application.
Memory pads	VDDIO_MEM	TBD (MDDR mode)	Memory chips are not included.
	VREF_MEM	100 ~ 250 (DDR mode)	
Total	-	550 ~ 900	-

Table 13: SiRFatlasⅣ Power Consumption in Typical Case

Power Consumption in Sleep Mode

In sleep mode, VDD_PDN, PLL, TSC and USB are shut down, and other powers are working. The power consumption data in this mode is shown in the table below. The testing conditions are:

- Ambient temperature: 25°C
- Application scenario: in sleep mode

Power	Voltage (V)	Current (uA)	Comments
VDD_PRE	1.3	<450	This value depends on application.
VDDIO	3.3	<30	This value depends on application. In this scenario, it is less than 30μA.
VDD_MEM VREF_MEM	1.8	<10 (MDDR mode)	Memory chips are not included. In this scenario, it is less than 10μA.
	2.5	<10 (DDR mode)	
VDD_LVR + VDDIO_RTC	3.3	15 - 30	-

Table 14: SiRFatlasⅣ Power Consumption in Sleep Mode

Power Consumption in Deep-Sleep Mode

In deep-sleep mode, only RTC is working, other powers are shut down. The power consumption data in this mode is shown in the table below. The testing conditions are as follows:

- Ambient temperature: 25°C
- Application scenario: in deep-sleep mode

Power	Voltage (V)	Current (μA)
VDD_LVR +VDDIO_RTC	3.3	15 - 30

Table 15: SiRFatlasⅣ Power Consumption in Deep-Sleep Mode

Power Budget in System Design

The following table shows the power budget in system design. Ambient temperature: -20°C to 70°C

Type	Power	Current Budget (mA)	Comments
Core	VDD_PRE	50	-
	VDD_PDN	1000	-
RTC	VDD_LVR	1	-
	VDDIO_RTC	1	-
PLL	VDDA_PLL1, VDDA_PLL2	10	-
	VDD_PLL	-	-
MEM	VDDIO_MEM	150	• When using normal DDR memory. • This budget only includes SiRFatlas Ⅳ, not including external memory chips.
		TBD	• When using mobile DDR memory. • This budget only includes SiRFatlas Ⅳ, not including external memory chips.
	VREF_MEM	0.005	• It is only necessary for SSTL2 and SSTL18 pad mode. • Only include the leakage of SiRFatlas Ⅳ, not including external memory chips.
TSC	VDD_TSC	0.5	-
	VDDA_TSC VDDIO_TSC	25	-
USB	VDDA3V3_USB	10	-
	VDDA2V5_USB	25	-
eFuse	VPROG	30	When eFuse is in programming mode.
I/O	VDDIO VDDIO_PLL	100	-

Table 16: Power Budget in System Design

AC Timing Characteristics

AC Operation Frequency

The following table lists the operating frequencies of SiRFatlasⅣ.

Part	Max. for 600MHz Parts
ARM clock	500
DSP clock	250
SYS clock	250
DDR SDRAM clock	166
Mobile DDR SDRAM clock	TBD
I/O clock	125

Table 17: Clock Frequencies (Unit: MHz)

Boundary Scan JTAG Interface AC Timing

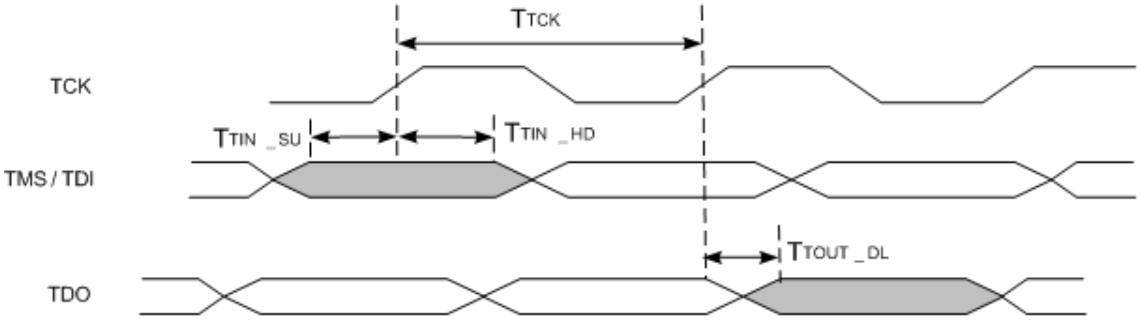


Figure 15: Boundary Scan JTAG Interface AC Timing Diagram

Symbol	Parameter	Min.	Typical	Max.
T_{TCK}	TCK cycle	200	-	-
T_{TIN_SU}	TDI, setup time to TCK rising edge	25	-	-
	TMS setup time from TCK rising edge	1.5	-	-
T_{TIN_HD}	TDI hold time to TCK rising edge	25	-	-
	TMS hold time from TCK rising edge	0.5	-	-
T_{TOUT_DL}	TDO output delay from TCK rising edge	75	80	85

Table 18: Boundary Scan JTAG Interface AC Timing Data (Unit: ns)

Memory Interface AC Timing

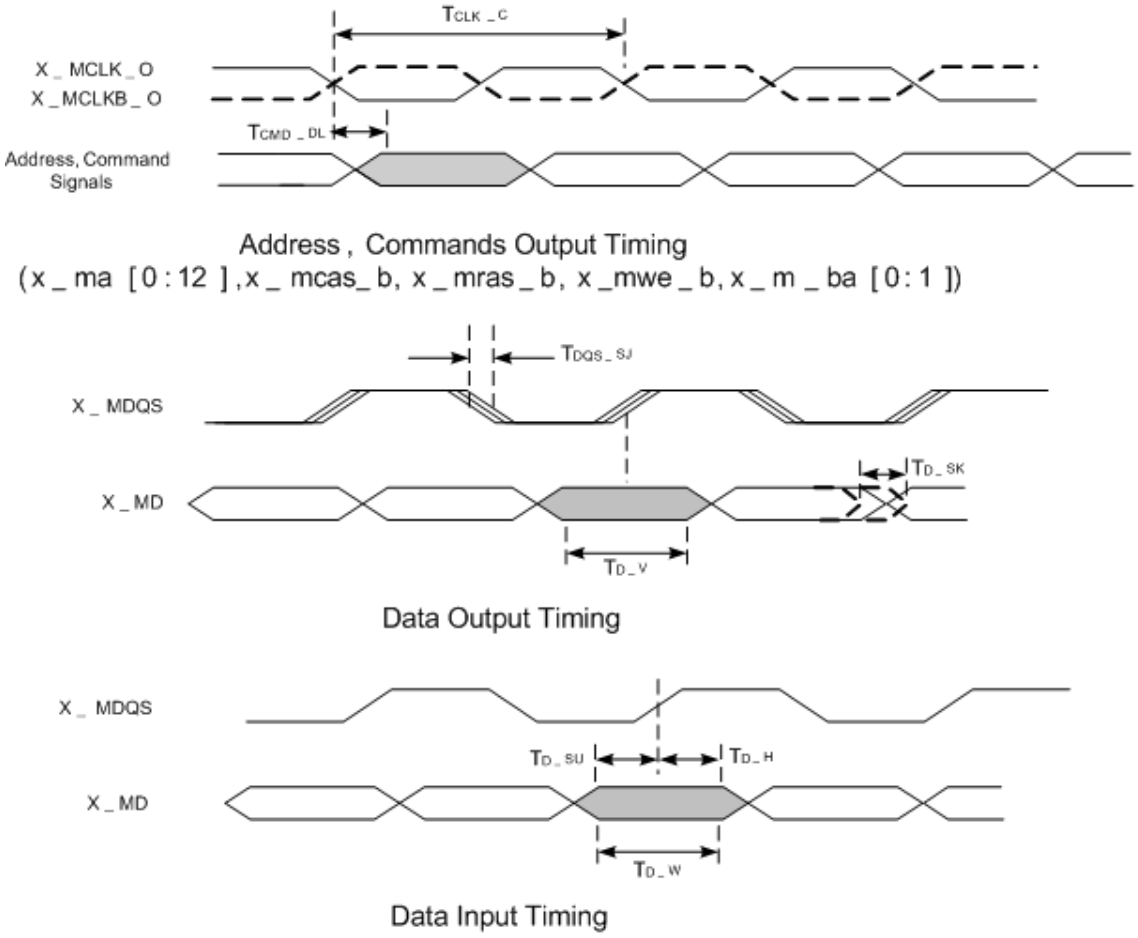


Figure 16: Memory Interface Key Timing

Symbol	Description	Min.	Typical	Max.
T_{CLK_C}	X_MCLK_O, X_MCLKB_O cycle	6	-	-
T_{CLK_J}	X_MCLK_O, X_MCLKB_O jitter	-	-	0.4
T_{CMD_DL}	Address, command signals output delay from MCLK	-	-	1.0
T_{DQS_SJ}	X_MDQS output jitter	-	-	0.4
T_{D_SK}	X_MD output skew	-	-	0.46
T_{D_V}	X_MD output valid window	2.0		-
T_{D_W}	X_MD input window request (setup time + hold time)	1.4	-	-

Table 19: Memory Interface AC Timing – DDR Mode (Unit: ns)

Symbol	Description	Min.	Typical	Max
T_{CLK_C}	X_MCLK_O, X_MCLKB_O cycle	TBD	-	-
T_{CLK_J}	X_MCLK_O, X_MCLKB_O jitter	-	-	0.4
T_{CMD_DL}	Address, command signals output delay from MCLK	-	-	TBD
T_{DQS_SJ}	X_MDQS output jitter	-	-	0.4
T_{D_SK}	X_MD output skew	-	-	TBD
T_{D_V}	X_MD output valid window	TBD	-	-
T_{D_W}	X_MD input window request (setup time + hold time)	TBD	-	-

Table 20: Memory Interface AC Timing – Mobile DDR Mode (Unit: ns)

Symbol	Description	Min.	Typical	Max.
T_{CLK_C}	X_MCLK_O, X_MCLKB_O cycle	TBD	-	-
T_{CLK_J}	X_MCLK_O, X_MCLKB_O jitter	-	-	0.4
T_{CMD_DL}	Address, command signals output delay from MCLK	-	-	TBD
T_{DQS_SJ}	X_MDQS output jitter	-	-	0.4
T_{D_SK}	X_MD output skew	-	-	TBD
T_{D_V}	X_MD output valid window	TBD		-
T_{D_W}	X_MD input window request (setup time + hold time)	TBD	-	-

Table 21: Memory Interface AC Timing – SSTL 18 Mode (Unit: ns)

SD0/1/2/3 Interface AC Timing

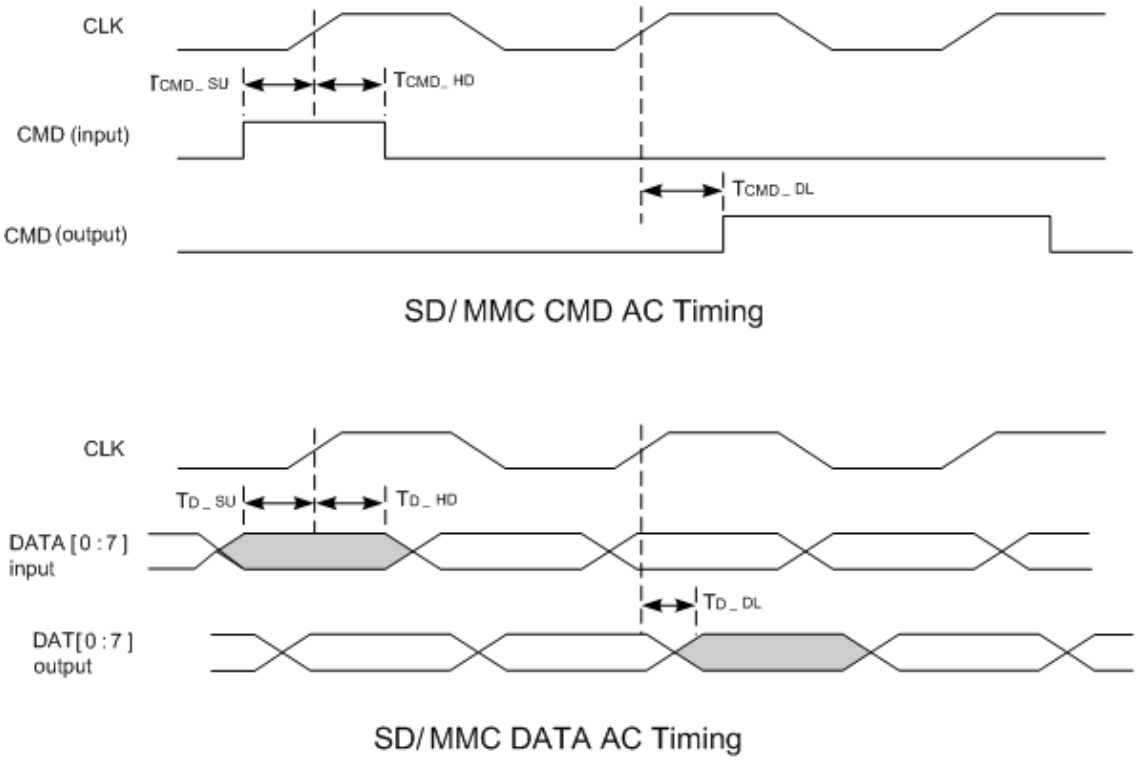


Figure 17: SD0/2, MMC AC Timing

Symbol	Parameter	Min.	Typical	Max.
T_{CMD_SU}	X_DF_ALE,SD0 CMD input setup time request	2.5	-	-
T_{CMD_HD}	X_DF_ALE,SD0 CMD input hold time request	0	-	-
T_{CMD_DL}	X_DF_ALE,SD0 CMD output delay	5.5		9.5
T_{D_SU}	X_DF_AD[0:7],SD0 data input setup time request	3	-	-
T_{D_HD}	X_DF_AD[0:7],SD0 data input hold time request	0	-	-
T_{D_DL}	X_DF_AD[0:7],SD0 data output delay	5		9.5

Table 22: SD Slot 0 AC Timing Data (Unit: ns)

Symbol	Parameter	Min.	Typical	Max.
T_{CMD_SU}	X_DF_RE,SD2 CMD input setup time request	3	-	-
T_{CMD_HD}	X_DF_RE,SD2 CMD input hold time request	0	-	-
T_{CMD_DL}	X_DF_RE,SD2 CMD output delay	5.5		9.5
T_{D_SU}	X_DF_AD[0:7] SD2 data input setup time request	3	-	-
T_{D_HD}	X_DF_AD[0:7] SD2 data input hold time request	0	-	
T_{D_DL}	X_DF_AD[0:7] SD2 data output delay	5.5		9.5

Table 23: SD Slot 2 AC Timing Data (Unit: ns)

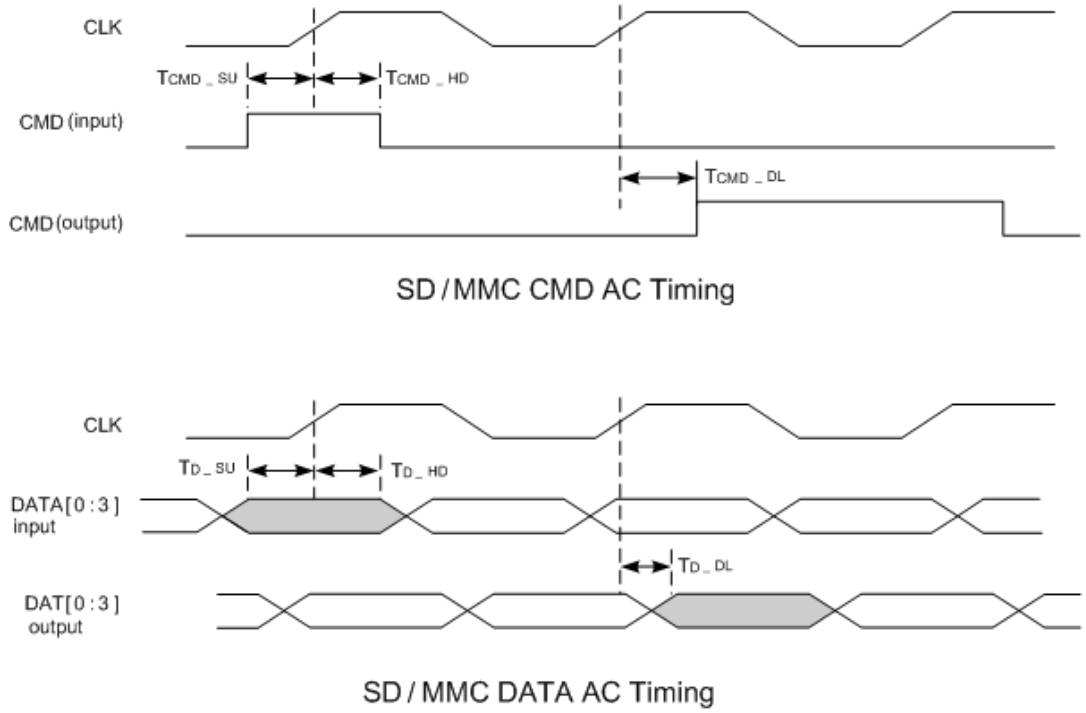


Figure 18: SD1/3, MMC AC Timing

Symbol	Parameter	Min.	Typical	Max.
T_{CMD_SU}	X_SD_CMD_1 input setup time request	3	-	-
T_{CMD_HD}	X_SD_CMD_1 input hold time request	0	-	-
T_{CMD_DL}	X_SD_CMD_1 output delay	7		10.5
T_{D_SU}	X_SD_DAT_1[0:3] data input setup time request	3	-	-
T_{D_HD}	X_SD_DAT_1[0:3] data input hold time request	0	-	-
T_{D_DL}	X_SD_DAT_1[0:3] data output delay	5.5		10

Table 24: SD Slot 1 AC Timing Data (Unit: ns)

Symbol	Parameter	Min.	Typical	Max.
T_{CMD_SU}	X_SD_CMD_3 input setup time request	2	-	-
T_{CMD_HD}	X_SD_CMD_3 input hold time request	0	-	-
T_{CMD_DL}	X_SD_CMD_3 output delay	6		10
T_{D_SU}	X_SD_DAT_3[0:3] data input setup time request	2	-	-
T_{D_HD}	X_SD_DAT_3[0:3] data input hold time request	0	-	-
T_{D_DL}	X_SD_DAT_3[0:3] data output delay	5		10

Table 25: SD Slot 3 AC Timing Data (Unit: ns)

NAND Flash Interface AC Timing

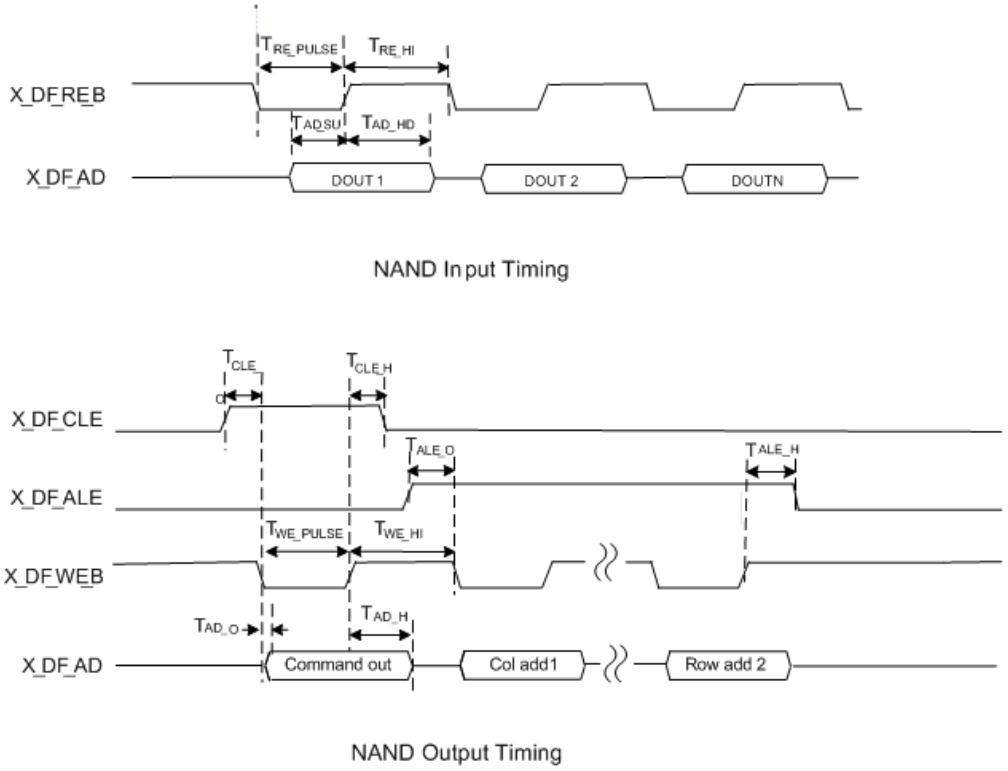


Figure 19: NAND Flash Interface AC Timing

Symbol	Parameter	Min.	Typical	Max.
T_{RE_PULSE}	X_DF_RE_B low pulse	-	(RD_PULSE+1)xT_{IOCLK}	-
T_{RE_HI}	X_DF_RE_B hi width between low pulses	-	(RD_WT_HI+1)xT_{IOCLK}	-
T_{AD_SU}	X_DF_AD setup time request when input	10.5	-	-
T_{AD_HD}	X_DF_AD hold time request when input	0	-	-
T_{WE_PULSE}	X_DF_WE_B low pulse	-	Command/address cycle:(WT_PULSE) xT_{IOCLK} Write data output cycle: (1+WT_PULSE) xT_{IOCLK}	-
T_{WE_HI}	X_DF_WE_B hi width between low pulses	-	Command/address cycle:(2+RD_WT_HI) xT_{IOCLK} Write data output cycle: (1+RD_WT_HI) xT_{IOCLK}	-
T_{AD_O}	X_DF_AD output time			4.5
T_{CLE_O}	X_DF_CLE output time	-	1xT_{IOCLK}	-

Symbol	Parameter	Min.	Typical	Max.
T_{ALE_O}	X_DF_ALE output time	-	$1xT_{IOCLK}$	-
T_{CLE_H}	X_DF_CLE output hold time	-	$(RD\_WT\_HI+1)xT_{IOCLK}$	-
T_{ALE_H}	X_DF_ALE output hold time	-	$(RD\_WT\_HI+1)xT_{IOCLK}$	-
T_{AD_H}	X_DF_ALE output hold time	-	$(RD\_WT\_HI)xT_{IOCLK}$	-

Table 26: NAND Flash Interface AC Timing Data (Unit: ns)

LCD Interface AC Timing

- Master mode

  When the LCD controller works in master mode, all pins are output.

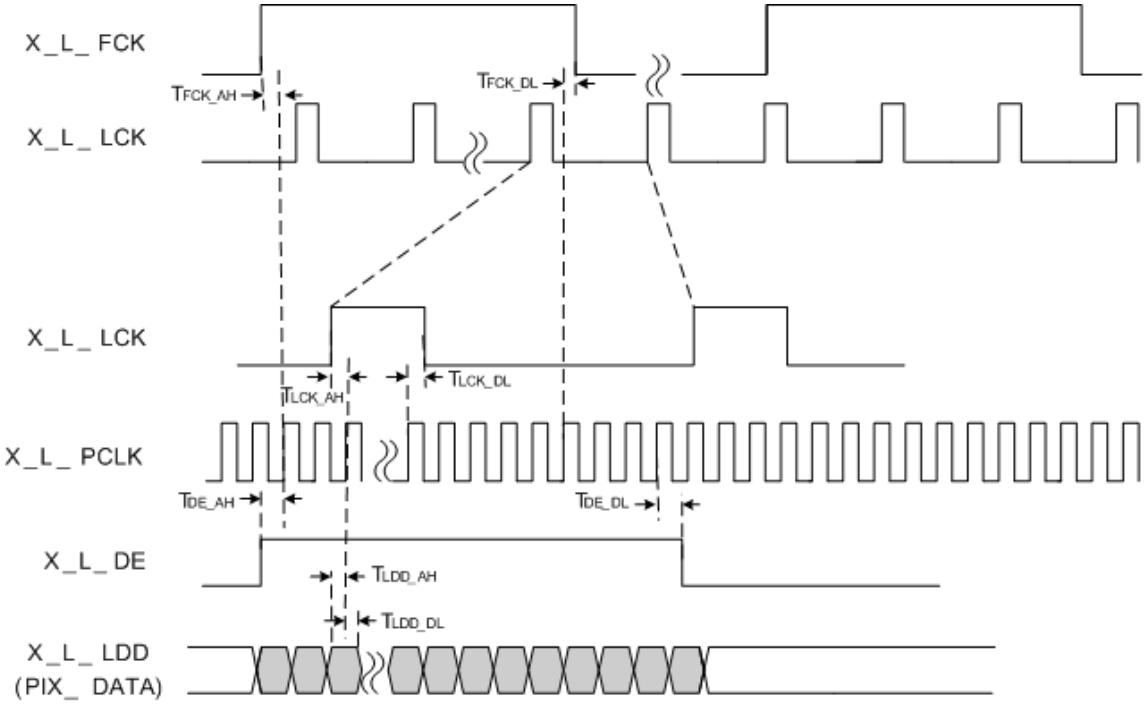


Figure 20: LCD Interface Timing Diagram in Master Mode

Symbol	Description	Value
T_{pclk}	Pix clock period	(Ratio+1) x Tsys
T_{FCK_AH}	X_L_FCK output ahead before X_L_PCLK	(Ratio-SYNC_DLY) x Tsys
T_{FCK_DL}	X_L_FCK output delay than X_L_PCLK	(SYNC_DLY+1) x Tsys
T_{LCK_AH}	X_L_LCK output ahead before X_L_PCLK	(Ratio-SYNC_DLY) x Tsys
T_{LCK_DL}	X_L_LCK output delay than X_L_PCLK	(SYNC_DLY+1) x Tsys

Symbol	Description	Value
T_{DE_AH}	X_L_DE output ahead before X_L_PCLK	(Ratio-SYNC_DLY) x Tsys
T_{DE_DL}	X_L_DE output delay than X_L_PCLK	(SYNC_DLY+1) x Tsys
T_{LDD_AH}	X_LDD output ahead before X_L_PCLK	Tpclk/2
T_{LDD_DL}	X_LDD output delay than X_L_PCLK	Tpclk/2

Table 27: LCD Interface AC Timing in Master Mode

- Slave mode

  When the LCD controller works in slave mode:

  - PIXCLK is input.
  - X_VSYNC and X_HSYNC can be input or output.
  - X_L_DE and X_LDD are output.

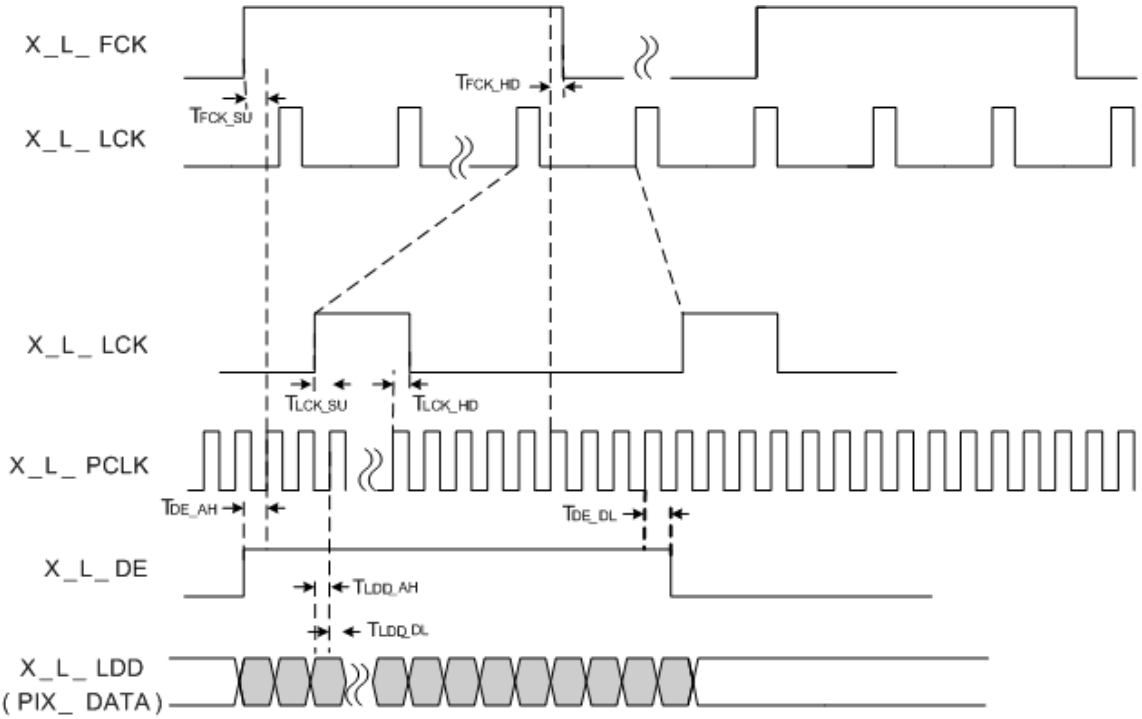


Figure 21: LCD Interface Timing in Slave Mode

Symbol	Description	Min.	Typical	Max.
T_{pclk}	Pix clock period.		37	-
T_{FCK_SU}	X_L_FCK setup time for X_L_PCLK when X_L_FCK is input.	5	-	-
T_{FCK_HD}	X_L_FCK hold time for X_L_PCLK when X_L_FCK is input.	5	-	-
T_{FCK_AH}	X_L_FCK output ahead before X_L_PCLK, when X_L_FCK is output.	-	Tpclk – (2+SYNC_DLY) x Tsys	-
T_{FCK_DL}	X_L_FCK output delay than X_L_PCLK when X_L_FCK is output.	-	(2+SYNC_DLY) x Tsys	-
T_{LCK_SU}	X_L_LCK setup time for X_L_PCLK when X_L_LCK is input.	5	-	-
T_{LCK_HD}	X_L_LCK hold time for X_L_PCLK when X_L_LCK is input.	5	-	-
T_{LCK_AH}	X_L_LCK output ahead before X_L_PCLK when X_L_LCK is output.	-	Tpclk – (2+SYNC_DLY) x Tsys	-
T_{LCK_DL}	X_L_LCK output delay than X_L_PCLK when X_L_LCK is output.	-	(2+SYNC_DLY) x Tsys	-
T_{DE_AH}	X_L_DE output ahead before X_L_PCLK.	-	Tpclk – (2+SYNC_DLY) x Tsys	-
T_{DE_DL}	X_L_DE output delay than X_L_PCLK.	-	(2+SYNC_DLY) x Tsys	-
T_{LDD_AH}	X_LDD output ahead before X_L_PCLK.	-	Tpclk/2	-
T_{LDD_DL}	X_LDD output delay than X_L_PCLK.	-	Tpclk/2	-

Table 28: LCD Interface AC Timing in Slave Mode (Unit: ns)

Audio Codec AC Timing

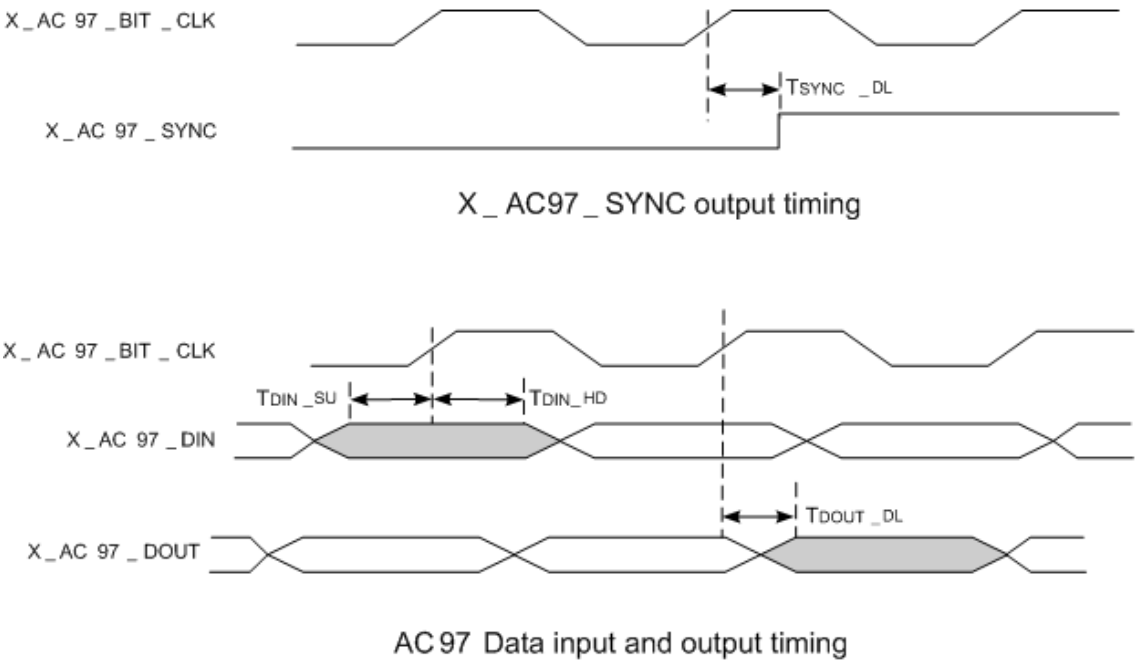


Figure 22: AC97 Interface AC Timing (AC97 Mode)

Symbol	Parameter	Min.	Typical	Max.
T_{SYNC_DL}	X_AC97_SYNC output delay from X_AC97_BIT_CLK rising edge	5.5	6.5	10
T_{DIN_SU}	X_AC97_DIN setup time to X_AC97_BIT_CLK rising edge	0.6	-	-
T_{DIN_HD}	X_AC97_DIN hold time from X_AC97_BIT_CLK rising edge	0.2	-	-
T_{DOUT_DL}	X_AC97_DOUT output delay from X_AC97_BIT_CLK rising edge	5.5	6.5	9

Table 29: AC97 Interface AC Timing Data (AC97 Mode) (Unit: ns)

VIP Interface AC Timing

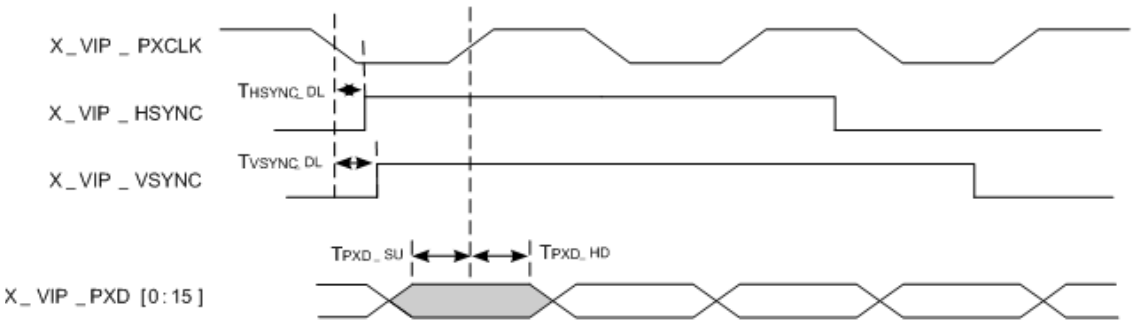


Figure 23: VIP Interface AC Timing (Camera Master Mode)

Symbol	Parameter	Min.	Typical	Max.
T_{PXCLK}	Pix clock period	-	2 x (PIXCLK_NUM+1) x TIOCLK	-
T_{PXD_SU}	X_VIP_PXD setup time from X_VIP_PXCLK falling edge	5.5	-	-
T_{PXD_HD}	X_VIP_PXD hold time from X_VIP_PXCLK falling edge	0	-	-
T_{HSYNC_DL}	X_VIP_HSYNC output delay time from X_VIP_PXCLK rising edge	-	At the falling edge of X_VIP_PXCLK	-
T_{VSYNC_DL}	X_VIP_VSYNC output delay time from X_VIP_PXCLK rising edge	-	At the falling edge of X_VIP_PXCLK	-

Table 30: VIP AC Timing Data (Camera Master Mode) (Unit: ns)

SPI Interface AC Timing

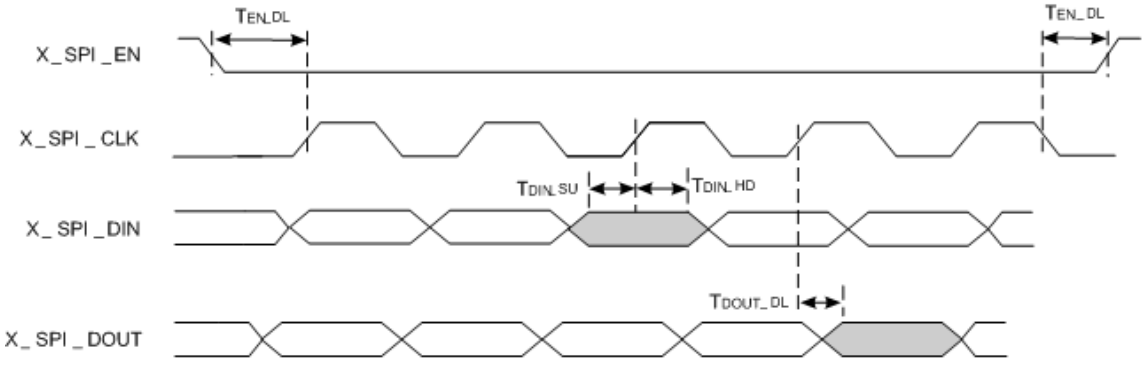


Figure 24: SPI Interface AC Timing (Master Mode)

Symbol	Parameter	Min.	Typical	Max.
T_{DIN_SU}	X_SPI_DIN setup time to X_SPI_CLK receive edge	1.9	-	-
T_{DIN_HD}	X_SPI_DIN hold time from X_SPI_CLK receive edge	0	-	-
T_{DOUT_DL}	X_SPI_DOUT output delay time from X_SPI_CLK transfer edge	-	At the transfer edge of X_SPI_CLK	-
T_{EN_DL}	X_SPI_EN output delay time to X_SPI_CLK transfer edge	1 x T_{SPI_CLK}	-	2 x T_{SPI_CLK}

Table 31: SPI AC Timing Data (Master Mode) (Unit: ns)

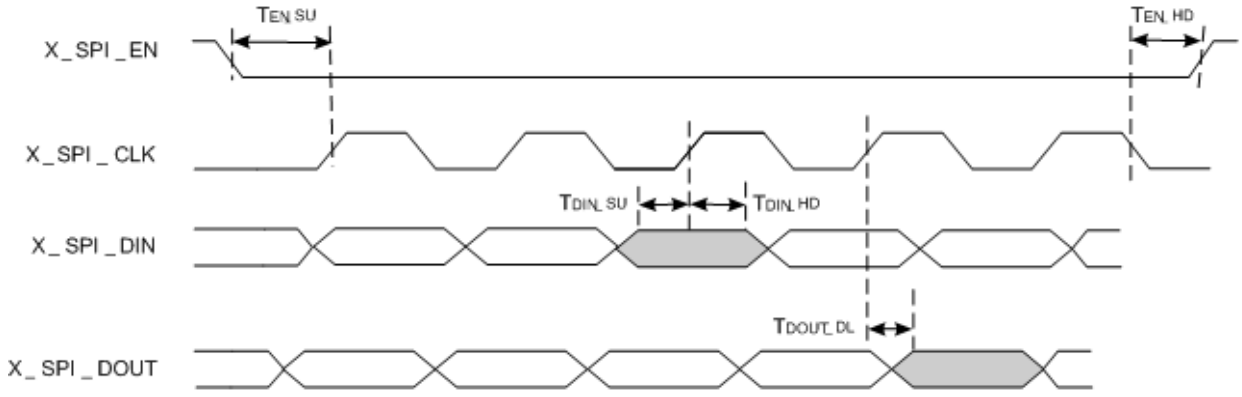


Figure 25: SPI Interface AC Timing (Slave Mode)

Symbol	Parameter	Min.	Typical	Max.
T_{DIN_SU}	X_SPI_DIN setup time to X_SPI_CLK receive edge	0	-	-
T_{DIN_HD}	X_SPI_DIN hold time from X_SPI_CLK receive edge	4 x T_{IOCLK}	-	-
T_{DOUT_DL}	X_SPI_DOUT output delay time from X_SPI_CLK transfer edge	4 x T_{IOCLK}		
T_{EN_SU}	X_SPI_EN setup time to X_SPI_CLK first edge	If DRV==CLK 4*Tioclk+0.5Tspi_clk If DRV!=CLK 4*Tioclk	-	-
T_{EN_HD}	X_SPI_EN hold time from X_SPI_CLK last edge	If DRV==CLK 4*Tioclk-0.5Tspi_clk If DRV!=CLK 4*Tioclk	-	-

Table 32: SPI AC Timing Data (Slave Mode) (Unit: ns)

I²C0 and I²C1 Interface AC Timing

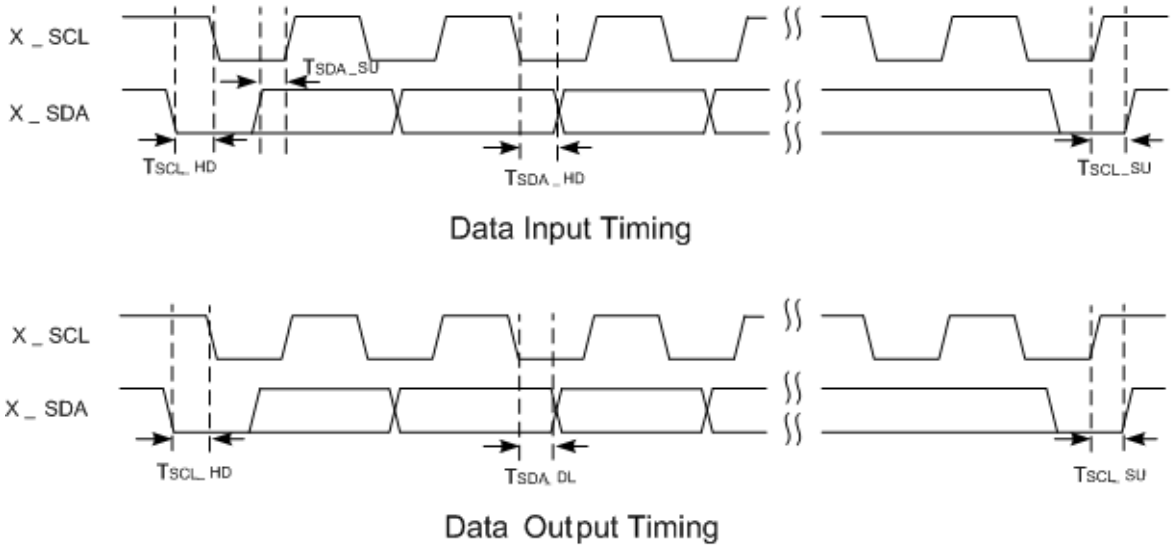


Figure 26: I²C Interface AC Timing Diagram

Symbol	Parameter	Min.	Typical	Max.
$F_{C(SCL\_0)}$	X_SCL_0 operating frequency (KHz)	-	F_{IOCLK}/(CLK_PERx5)	400
$T_{SDA\_0\_DL}$	X_SDA_0 output delay time after X_SCL_0 falling edge (µs)	-	T_{IOCLK} x (SDA_DELAY_REG+4)	-
$T_{SDA\_0\_SU}$	X_SDA_0 setup time to X_SCL_0 rising edge (ns)	250	-	-
$T_{SDA\_0\_HD}$	X_SDA_0 hold time from X_SCL_0 rising edge (ns)	0	-	-
$T_{SCL\_0\_HD}$	X_SCL_0 hold time after X_SDA_0 falling edge (µs)	-	T_{IOCLK} x CLK_PER	-
$T_{SCL\_0\_SU}$	X_SCL_0 setup time before X_SDA_0 rising edge (µs)	-	T_{IOCLK} x (CLK_PER + 2)	-

Table 33: I²C0 AC Timing Data (Master Mode)

Symbol	Parameter	Min.	Typical	Max.
$F_{C(SCL\_1)}$	X_SCL_1 operating frequency (KHz)	-	F_{IOCLK} / (CLK_PER x 5)	400
$T_{SDA\_1\_DL}$	X_SDA_1 output delay time after X_SCL_0 falling edge (us)	-	T_{IOCLK} x (SDA_DELAY_REG+4)	-
$T_{SDA\_1\_SU}$	X_SDA_1 setup time to X_SCL_1 rising edge (ns)	250	-	-
$T_{SDA\_1\_HD}$	X_SDA_1 hold time from X_SCL_1 falling	0	-	-

Symbol	Parameter	Min.	Typical	Max.
	edge (ns)			
$T_{SCL\_1\_HD}$	X_SCL_1 hold time after X_SDA_1 falling edge (µs)	-	T_{IOCLK} x CLK_PER	-
$T_{SCL\_1\_SU\_S}$	X_SCL_1 setup time before X_SDA_1 rising edge (µs)	-	T_{IOCLK} x (CLK_PER + 2)	-

Table 34: I^2C1 AC Timing Data (Master Mode)

REVISION HISTORY

Version	Date	Author	Comments
Rev 1.0	5/15.2009	Zhanqiang Su	Initial Release

ADDITIONAL INFORMATION

Additional technical information including Application Notes are available through the Customer Zone on the SiRF web site at http://www.sirf.com

ORDERING INFORMATION

Part Number	Marking	Package	Frequency	Dimension (mm)	Packing	Core Current Leakage
AT8401	AT840	TFBGA-292	500MHz	12 x 12	Tray	Commercial grade

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