Version : 0.4

Electrophoretic display controller

SPECIFICATION

MODEL NAME: PVI-6001A(P-TFBGA-177)

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐PVI's Confirmation

Confirmed By _____

Prepared By _____

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Date : JAN/08/2007

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1. GENERAL DESCRIPTION

The PVI-6001A display controller is a display controller for a TFT (thin film transistor) active matrix Electrophoretic display. It is part of a reference system electronics design designed for Electrophoretic displays.

The PVI-6001A is suitable for 800 x 600 pixels, and has 1-bit and 2-bit display capabilities. It has an aspect ratio of 4:3, portrait or landscape. The PVI-6001A drives the source and gate drivers. It has an 8-bit parallel asynchronous data bus and uses external SRAM memory to store the display data. It composes the required display waveforms to generate images on the displays using an external Look-Up-Table (flash memory).

The IC is designed for an electrophoretic display used with a reference system electronics design describing the necessary support electronics, and operating firmware defining key parameters of the display operation

This specification describes the performance and key electrical specification of the PVI-6001A display controller.

2. FEATURES

* TFT electrophoretic display controller
* 800 x 600 pixels
* 4:3 aspect ratio, portrait or landscape.
* Uses two clock frequencies to reduce power. (33Mhz and 70 KHz)
* Two low power modes available. (Sleep and standby).
* Built-in buffer for rotation of orientation. (Portrait or landscape).
* Black and White or 4 levels grayscale mode.
* Capable of partial write operations in rectangular regions indicated by two apexes.
* Industrial temperature range.
*8- bit parallel bi-directional asynchronous interface, with handshake protocol.
* Maximum communication speed of host interface is 10 Mbytes/sec.
* One or more controllers can be connected to the host bus.
* Uses I2c master interface for temperature sensor.
* Uses double external low power SRAM (70 nsec access time).
* Uses external Flash Rom as Look-Up-Table (90 nsec access time).
* Available in a 177 pins lead free P-TFBGA package.

3. QUICK REFERENCE DATA

Function : Electrophoretic display controller
(electronic ink display; E-Ink display)

Type Number : PVI-6001A
VDD : 2.7 ~ 3.6 V
Operating Ambient Temp : 85 ~ -20 ℃
Process : CMOS 0.35um
Package : P-TFBGA-177 lead free
Size : 13 x 13 mm
Ball Spacing : 0.8 mm

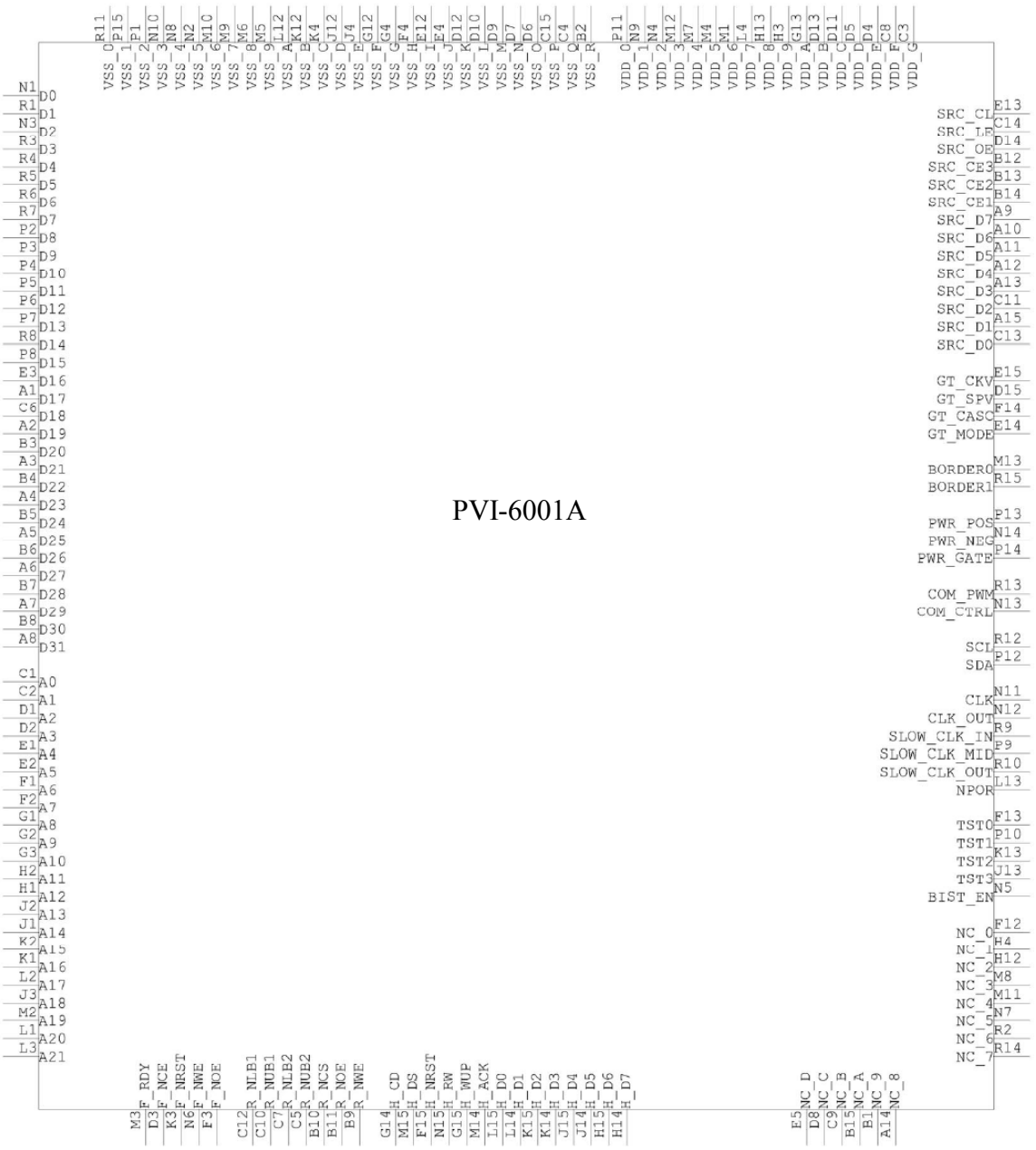


Figure 3.1 Symbol PVI-6001A

4. BLOCK DIAGRAM PVI-6001A

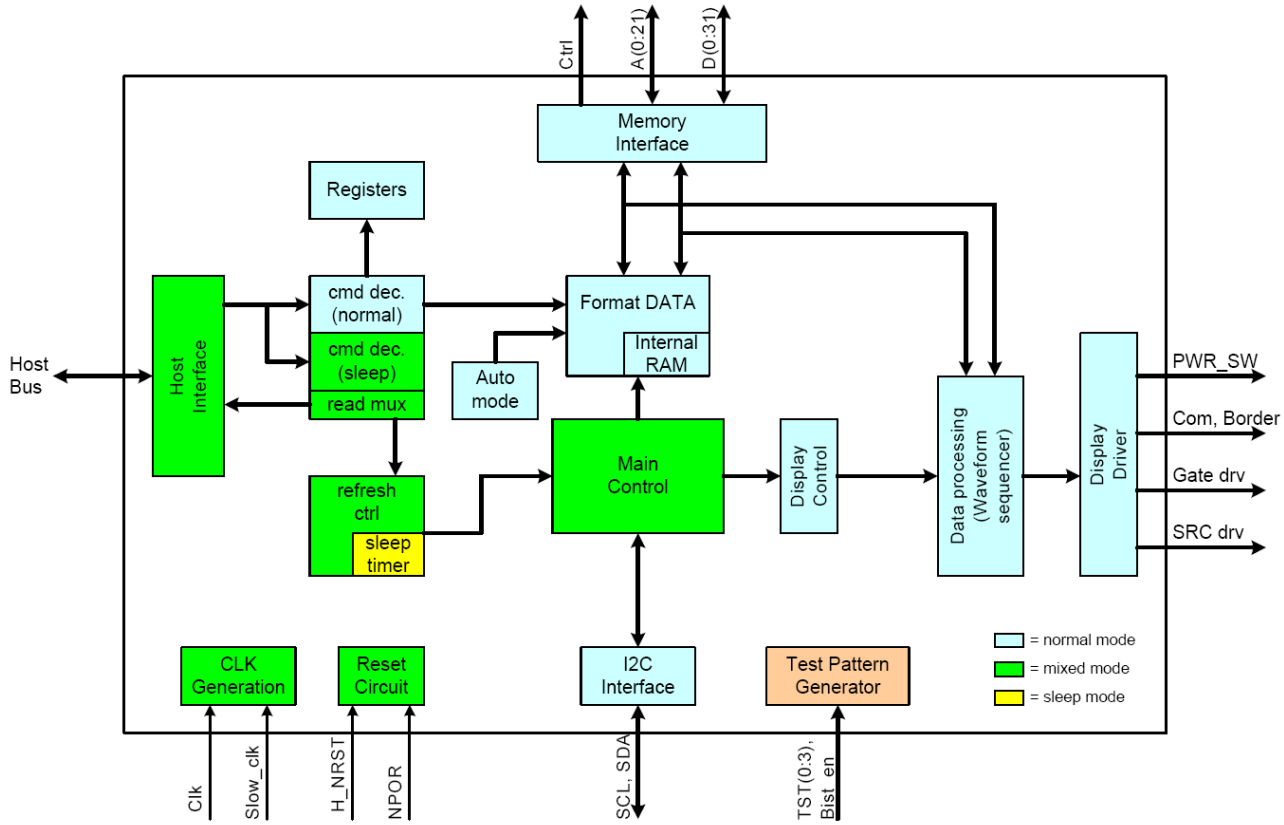


Figure 4.1 Block diagram PVI-6001A

5. PINNING

Name	Pin number	Type	Description
Clock circuit			
CLK	N11	Clock input	Clock_input(+)
CLK_OUT	N12	Clock output	Clock_output(-)
SLOW_CLK_IN	R9	In,COMS-schmitt	Slow_clock_input(+)
SLOW_CLK_MID	P9	Output	Slow_clock_middle
SLOW_CLK_OUT	R10	Output	Slow_clock_output(-)
NPOR	L13	In,CMOS-schmitt	Power Up reset
SRAM & Flash ROM			
D0	N1	I/O,CMOS	Data bus 32 bits
D1	R1	I/O,CMOS	Data bus 32 bits
D2	N3	I/O,CMOS	Data bus 32 bits
D3	R3	I/O,CMOS	Data bus 32 bits
D4	R4	I/O,CMOS	Data bus 32 bits
D5	R5	I/O,CMOS	Data bus 32 bits
D6	R6	I/O,CMOS	Data bus 32 bits
D7	R7	I/O,CMOS	Data bus 32 bits
D8	P2	I/O,CMOS	Data bus 32 bits
D9	P3	I/O,CMOS	Data bus 32 bits
D10	P4	I/O,CMOS	Data bus 32 bits
D11	P5	I/O,CMOS	Data bus 32 bits
D12	P6	I/O,CMOS	Data bus 32 bits
D13	P7	I/O,CMOS	Data bus 32 bits
D14	R8	I/O,CMOS	Data bus 32 bits
D15	P8	I/O,CMOS	Data bus 32 bits
D16	E3	I/O,CMOS	Data bus 32 bits
D17	A1	I/O,CMOS	Data bus 32 bits
D18	C6	I/O,CMOS	Data bus 32 bits
D19	A2	I/O,CMOS	Data bus 32 bits
D20	B3	I/O,CMOS	Data bus 32 bits
D21	A3	I/O,CMOS	Data bus 32 bits
D22	B4	I/O,CMOS	Data bus 32 bits
D23	A4	I/O,CMOS	Data bus 32 bits
D24	B5	I/O,CMOS	Data bus 32 bits
D25	A5	I/O,CMOS	Data bus 32 bits
D26	B6	I/O,CMOS	Data bus 32 bits
D27	A6	I/O,CMOS	Data bus 32 bits
D28	B7	I/O,CMOS	Data bus 32 bits
D29	A7	I/O,CMOS	Data bus 32 bits
D30	B8	I/O,CMOS	Data bus 32 bits
D31	A8	I/O,CMOS	Data bus 32 bits
A0	C1	Out,CMOS	Address bus 22bits
A1	C2	Out,CMOS	Address bus 22bits
A2	D1	Out,CMOS	Address bus 22bits
A3	D2	Out,CMOS	Address bus 22bits
A4	E2	Out,CMOS	Address bus 22bits

A5	E2	Out,CMOS	Address bus 22bits
A6	F1	Out,CMOS	Address bus 22bits
A7	F2	Out,CMOS	Address bus 22bits
A8	G1	Out,CMOS	Address bus 22bits
A9	G2	Out,CMOS	Address bus 22bits
A10	G3	Out,CMOS	Address bus 22bits
A11	H2	Out,CMOS	Address bus 22bits
A12	H1	Out,CMOS	Address bus 22bits
A13	J2	Out,CMOS	Address bus 22bits
A14	J1	Out,CMOS	Address bus 22bits
A15	K2	Out,CMOS	Address bus 22bits
A16	K1	Out,CMOS	Address bus 22bits
A17	L2	Out,CMOS	Address bus 22bits
A18	J3	Out,CMOS	Address bus 22bits
A19	M2	Out,CMOS	Address bus 22bits
A20	L1	Out,CMOS	Address bus 22bits
A21	L3	Out,CMOS	Address bus 22bits
F_RDY	M3	In,CMOS	Flash control ready not busy
F_NCE	D3	Out,CMOS	Flash control chip enable
F_NRST	K3	Out,CMOS	Flash control nreset
F_NWE	N6	Out,CMOS	Flash control write enable
F_NOE	F3	Out,CMOS	Flash control output enable
R_NLB1	C12	Out,CMOS	SRAM control byte select 0
R_NUB1	C10	Out,CMOS	SRAM control byte select 1
R_NLB2	C7	Out,CMOS	SRAM control byte select 2
R_NUB2	C5	Out,CMOS	SRAM control byte select 3
R_NCS	B10	Out,CMOS	SRAM control chip select
R_NOE	B11	Out,CMOS	SRAM control output enable
R_NWE	B9	Out,CMOS	SRAM control write enable
Display Source Driver			
SRC_D0	C13	Out,CMOS	Source driver data bus(8bits)
SRC_D1	A15	Out,CMOS	Source driver data bus(8bits)
SRC_D2	C11	Out,CMOS	Source driver data bus(8bits)
SRC_D3	A13	Out,CMOS	Source driver data bus(8bits)
SRC_D4	A12	Out,CMOS	Source driver data bus(8bits)
SRC_D5	A11	Out,CMOS	Source driver data bus(8bits)
SRC_D6	A10	Out,CMOS	Source driver data bus(8bits)
SRC_D7	A9	Out,CMOS	Source driver data bus(8bits)
SRC_CE1	B14	Out,CMOS	Source driver chip enable 1
SRC_CE2	B13	Out,CMOS	Source driver chip enable 2
SRC_CE3	B12	Out,CMOS	Source driver chip enable 3
SRC_OE	D14	Out,CMOS	Source driver output enable
SRC_LE	C14	Out,CMOS	Source driver latch enable
SRC_CL	E13	Out,CMOS	Source driver Clock
Display Gate Driver			
GT_CKV	E15	Out,CMOS	Gate driver clock
GT_SPV	D15	Out,CMOS	Gate driver start pulse
GT_CASC	F14	Out,CMOS	Gate driver cascade select
GT_MODE	E14	Out,CMOS	Gate driver mode select

Display Control Signals			
BORDER0	M13	Out,CMOS	Display border control signal
BORDER1	R15	Out,CMOS	Display border control signal
PWR_POS	P13	Out,CMOS	Positive voltage supply on
PWR_NEG	N14	Out,CMOS	Negative voltage supply on
PWR_GATE	P14	Out,CMOS	Gate voltage on
COM_PWM	R13	Out,CMOS	Display common pwm out
COM_CTRL	N13	Out,CMOS	Display common switch
Host Interface			
H_CD	G14	In LVTTL,schmitt	Host interface Command/not data
H_DS	M15	In LVTTL,schmitt	Host interface device select
H_NRST	F15	In LVTTL,schmitt	Host interface reset low active
H_RW	N15	In LVTTL,schmitt	Host interface read/not write
H_WUP	G15	In LVTTL,schmitt	Host interface wake up
H_ACK	M14	Tri-state out CMOS	Host interface acknowledge
H_D0	L15	I/O LVTTL	Host interface data bus(8bits)
H_D1	L14	I/O LVTTL	Host interface data bus(8bits)
H_D2	K15	I/O LVTTL	Host interface data bus(8bits)
H_D3	K14	I/O LVTTL	Host interface data bus(8bits)
H_D4	J15	I/O LVTTL	Host interface data bus(8bits)
H_D5	J14	I/O LVTTL	Host interface data bus(8bits)
H_D6	H15	I/O LVTTL	Host interface data bus(8bits)
H_D7	H14	I/O LVTTL	Host interface data bus(8bits)
I2C			
SCL	R12	I/O LVTTL Schmitt	I2C clock
SDA	P12	I/O LVTTL Schmitt	I2C data
Others			
TST0	F13	In CMOS	Select test mode(normal=’0’)
TST1	P10	In CMOS	Select test mode(normal=’0’)
TST2	K13	In CMOS	Select test mode(normal=’0’)
TST3	J13	In CMOS	Select auto mode(normal=’0’)
BIST_EN	N5	In CMOS	Chip memory mode(normal=’0’)
Not connected			
n.c.	A14		Not connected
n.c.	B1		Not connected
n.c.	B15		Not connected
n.c.	C9		Not connected
n.c.	D8		Not connected
n.c.	E5		Not connected
n.c.	F12		Not connected
n.c.	H4		Not connected
n.c.	H12		Not connected
n.c.	M8		Not connected
n.c.	M11		Not connected
n.c.	N7		Not connected
n.c.	R2		Not connected
n.c.	R14		Not connected

Power pins			
VDD	C3		+3.0V
VDD	C8		+3.0V
VDD	D4		+3.0V
VDD	D5		+3.0V
VDD	D11		+3.0V
VDD	D13		+3.0V
VDD	G13		+3.0V
VDD	H3		+3.0V
VDD	H13		+3.0V
VDD	L4		+3.0V
VDD	M1		+3.0V
VDD	M4		+3.0V
VDD	M7		+3.0V
VDD	M12		+3.0V
VDD	N4		+3.0V
VDD	N9		+3.0V
VDD	P11		+3.0V
GND			
VSS	B2		GND
VSS	C4		GND
VSS	C15		GND
VSS	D6		GND
VSS	D7		GND
VSS	D9		GND
VSS	D10		GND
VSS	D12		GND
VSS	E4		GND
VSS	E12		GND
VSS	F4		GND
VSS	G4		GND
VSS	G12		GND
VSS	J4		GND
VSS	J12		GND
VSS	K4		GND
VSS	K12		GND
VSS	L12		GND
VSS	M5		GND
VSS	M6		GND
VSS	M9		GND
VSS	M10		GND
VSS	N2		GND
VSS	N8		GND
VSS	N10		GND
VSS	P1		GND
VSS	P15		GND
VSS	R11		GND

Table 5.1 Pinning

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage						
V_{DD}	DC Supply voltage	V_{SS} =0V	-0.3V		+5.0	V
Pin Voltage						
V_{IN}	DC Input voltage	V_{SS} =0V	-0.3		VDD+0.3	V
V_{OUT}	DC Output voltage	V_{SS} =0V	-0.3		VDD+0.3	V
DC input current(max current input pin)						
I_{IN}	DC input current	V_{SS} =0V	-10		+10	mA
Temperature						
T_{STG}	Storage temperature		-40		+125	℃

Table 6.1 Absolute maximum ratings

6.2 Recommended operating range

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
V_{DD}	DC Supply voltage	V_{SS}=0V	2.7	3.0	3.6	V
DC input voltage						
V_{IN}	DC input voltage	V_{SS}=0V	0		V_{DD}	V
Temperature						
TJ	Junction temperature		-5		100	℃
Tamb	Ambient temperature		-20		85	℃
Clock frequency						
FCLK	Clock frequency		32.5	33	33.5	Mhz
FSLOWCLK	Slow clock frequency		60	70	80	Khz
DCLK	Duty cycle clock		40	50	60	%
DSLOWCLK	Duty cycle slow clock		20	50	80	%

Table 6.2 Recommended operating range

6.3 DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply Current						
I_{DD}	Normal mode supply current	V_{DD}=3.0V		40	50	mA
I_{SLEEP}	Sleep mode supply current	V_{DD}=3.0V		400	600	μA
$I_{STANDBY}$	Standby mode supply current	V_{DD}=3.0V		0.1	1	μA

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
Input voltage							
V_{IH}	High level input voltage						
		LVTTL		2.0			V
		LVTTL Schmitt-trigger		2.0			V
		CMOS		$0.8V_{DD}$			V
		CMOS Schmitt-trigger		$0.8V_{DD}$			V
V_{IL}	Low level input current						V
		LVTTL				0.8	V
		LVTTL Schmitt-trigger				0.8	V
		CMOS				0.2 V_{DD}	V
		CMOS Schmitt-trigger				0.2 V_{DD}	V
I_{IH}	High level input current		V_{IN} =V_{DD}	-10		10	μA
I_{IL}	Low level input current		V_{IN} =V_{SS}	-10		10	μA
I_{OZ}	High impedance leakage current		Vout = V_{DD} or V_{SS}	-10		10	μA
V_H	Schmitt-trigger hysteresis voltage						
		LVTTL			0.5		V
		LVTTL Schmitt-trigger			0.5		V
Output voltage							
V_{OH}	High level output voltage		I_{OH} = -4mA	2.4			
			I_{OH} = -1 μA	V_{DD} –0.05			
V_{OL}	Low level output voltage		I_{OH} = 4mA			0.4	V
			I_{OH} = 1 μA			V_{SS} +0.05	V

Table 6.3 DC characteristics

6.4 AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input capacitance						
C_{INPUT}					10	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Reset(NPOR)						
t_{reset}	Minimum length NPOR reset		40			ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SRAM & Flash interface						
t_{rise_mem}	Rise time memory I/O	C_{pin} =15pF		3.3		nsec
t_{fall_mem}	Fall time memory I/O	C_{pin} =15pF		3.4		nsec

Note: See also timing memory interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Display(Source, gate and control)						
$t_{rdisplay}$	Rise time display outputs	C_{pin} =15pF		3.3		nsec
$t_{fdisplay}$	Fall time display outputs	C_{pin} =15pF		3.4		nsec
t_{spv}	Length GT_SPV pulse(low)			60		μ sec
t_{ckv}	Period GT_CKV pulse		10.2	33	89	μ sec
f_{cl}	Frequency SRC_CL pulse			16.7		MHz
t_{le}	Length SRC_LE pulse			30		nsec
D_{PWM}	Duty cycle pwm output		0		100	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host bus						
t_{rise_host}	Rise time host bus	C_{pin} =15pF		3.3		nsec
t_{fall_host}	Fall time host bus	C_{pin} =15pF		3.4		nsec

Note: See also timing host bus interface

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I2C						
f_{SCL}	Clock frequency			400		nsec
f_{fI2C}	Fall time I2C outputs	C_{pin} =15pF		2*		nsec
t_{ri2c}	Rise time I2C outputs			N.A.*		
I_{inI2C}	Maximum input current				4	mA

Table 6.4 AC characteristics

* Depends on bus load and external pull up resistor

7. TIMING SPECIFICATION.

7.1 SRAM memory interface

The SRAM memory interface uses a 32 x 64kbit memory interface. Although the address bus is 22 bits wide, only the lower 16 address bits (A0..A15) are used for the SRAM.

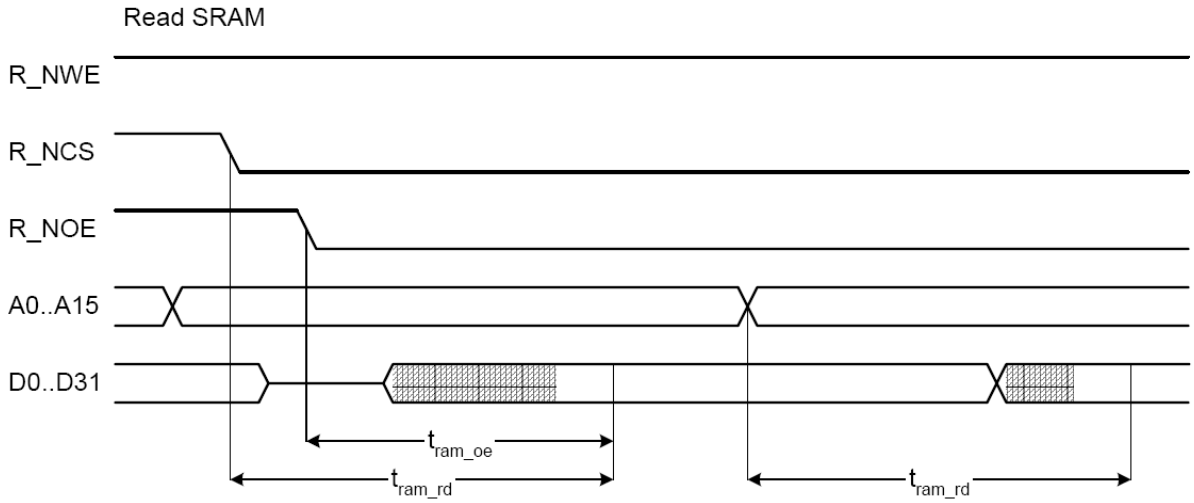


Figure 7.1 Timing read SRAM

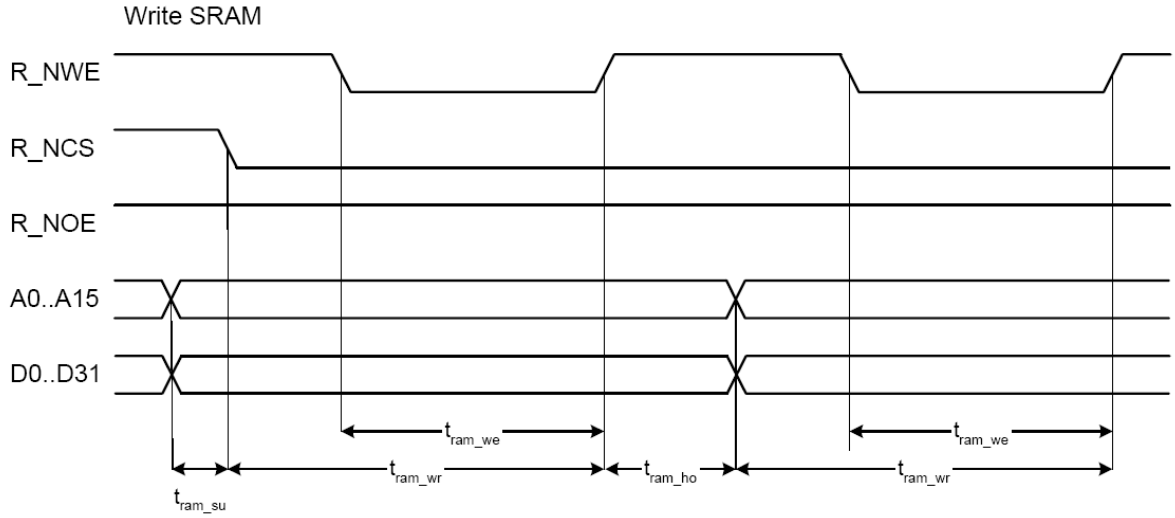


Figure 7.2 Timing write SRAM

Symbol	Parameter	Min	Typ	Max	Unit
f_{ram_rd}	Access time read for valid output	75			nsec
f_{ram_oe}	Output enable to valid output	45			nsec
f_{ram_wr}	Access time write	85			nsec
f_{ram_we}	Write pulse width	55			nsec
f_{ram_su}	Setup up time data and address	0			nsec
f_{ram_ho}	Hold time data and address			30	nsec

Table 7.1 Timing SRAM

Note: SRAM interface is designed for low power SRAM memories(70 nsec access time).

7.2 FLASH ROM memory interface.

The FLASH ROM memory interface uses an 8 x 4Mbit memory interface. Although the data bus is 32 bits wide, only the lower 8 data bits (D0..D7) are used for the FLASH ROM.
The memory interface is maximum 22 bits wide but can also be used with smaller devices. Minimum required size is 8x 64kBit.

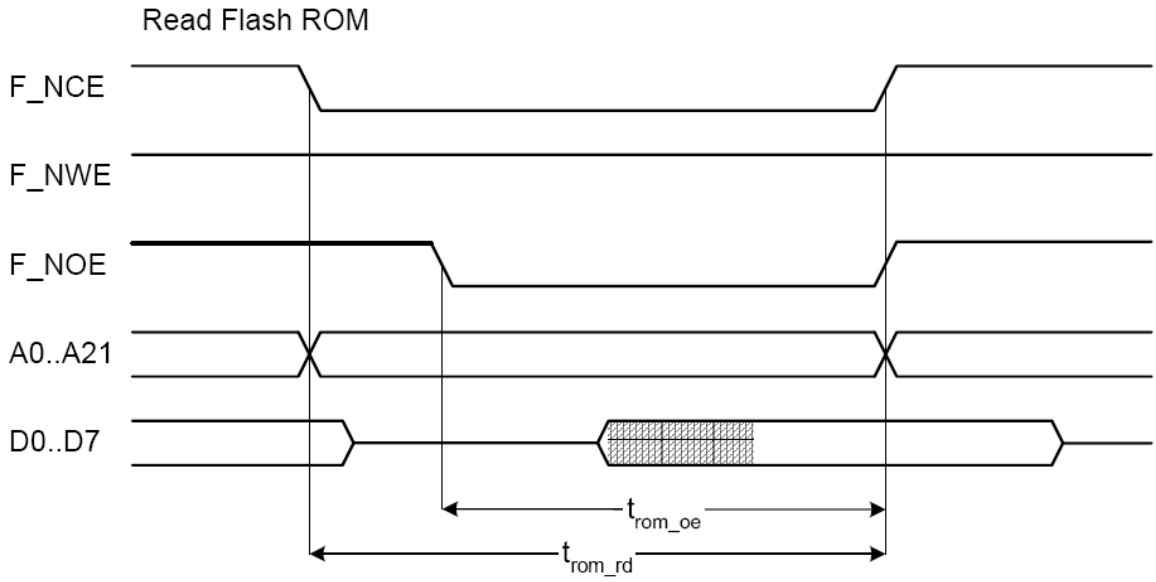


Figure 7.3 Timing read Flash ROM

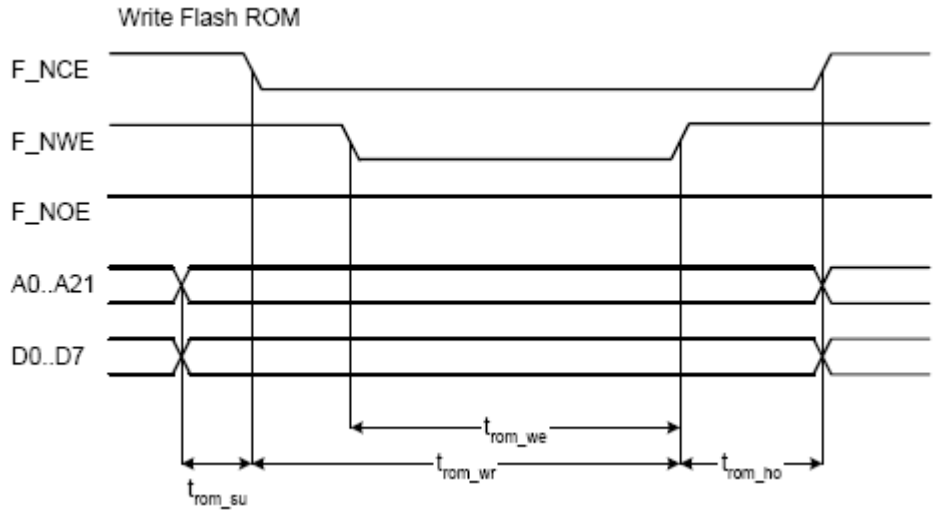


Figure 7.4 Timing write Flash ROM

Symbol	Parameter	Min	Typ	Max	Unit
f_{rom_rd}	Access time read for valid output	100			nsec
f_{rom_oe}	Output enable to valid output	70			nsec
f_{rom_wr}	Access time write	115			nsec
f_{rom_we}	Nominal access time write	85			nsec
f_{rom_su}	Set up time for data write	0			nsec
f_{rom_ho}	Hold time data of data write			30	nsec

Table 7.2 Timing Flash ROM

Note: FLASH interface is designed for low voltage Flash memories (90 nsec access time)

7.3 Timing host interface

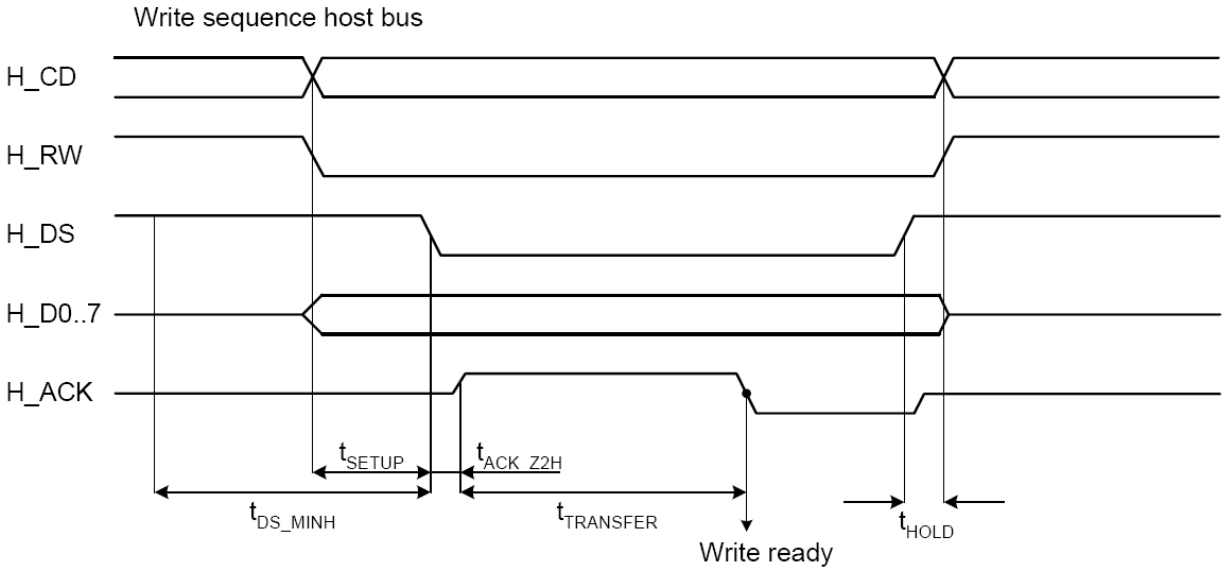


Figure 7.5 Write sequence host bus

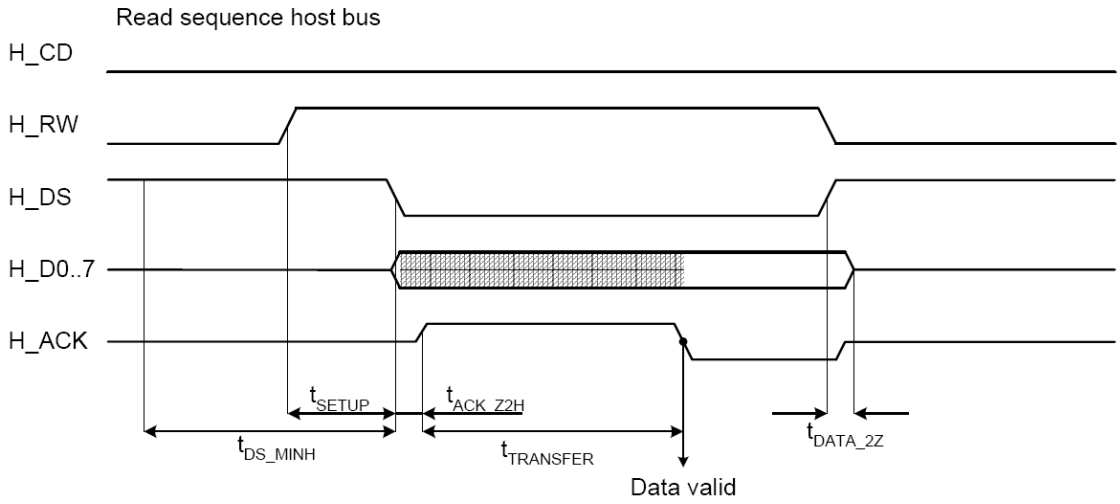


Figure 7.6 Read sequence host bus

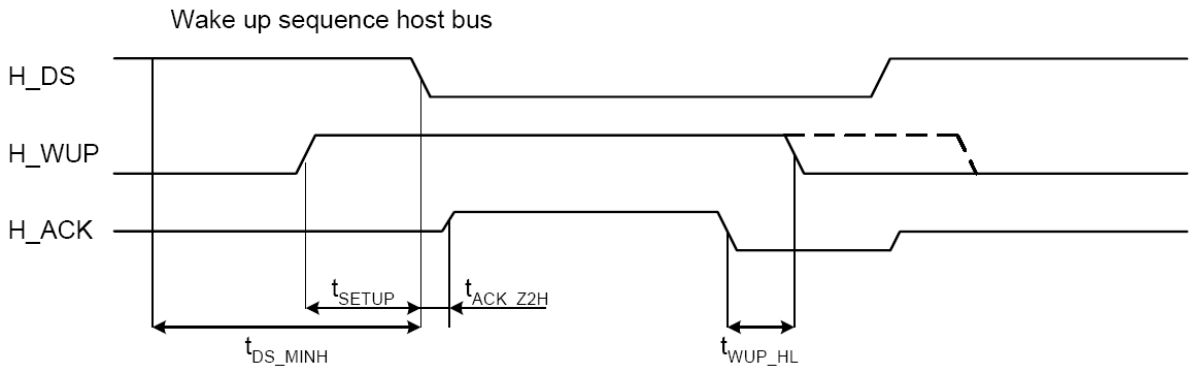


Figure 7.7 Wake up sequence host bus

Symbol	Parameter	Min	Typ	Max	Unit
t_{DS_MINH}	Minimum time high H_DS	35			nsec
$t_{TRANSFER}$	Transfer time data	60	75		nsec
t_{SETUP}	Setup time host bus	20			nsec
t_{ACK_Z2H}	Minimum response time of acknowledge			10*	nsec
t_{HOLD}	Hold time host bus	0			nsec
t_{DATA_2Z}	Minimum release time of data bus			10	nsec
t_{WUP_HL}	Minimum hold time WUP during wake-up	35			nsec

Table 7.3 Timing host bus

* Response time is load dependent.(15pF).

It's recommended to use pull up resistor of 100K to ensure a normal high position.

8. HOST PROTOCOL
This chapter covers the specifications of the host interface.

8.1 Connection and overview.
The controller is connected to the host via an 8-bit parallel interface. The interface transfer speed is max 10 MBytes/sec. The host communication protocol is an asynchronous interface with handshake. The host bus is designed to support multiple controllers connected to a single host bus.

Selection of the device is done with a data strobe signal (H_DS). The protocol uses a signal (H_RW) to determine the direction of the host bus (read or write) and a separate signal to distinguish between commands and data (H_CD).
The interface signals between the host and controller are listed in Table 8.1.

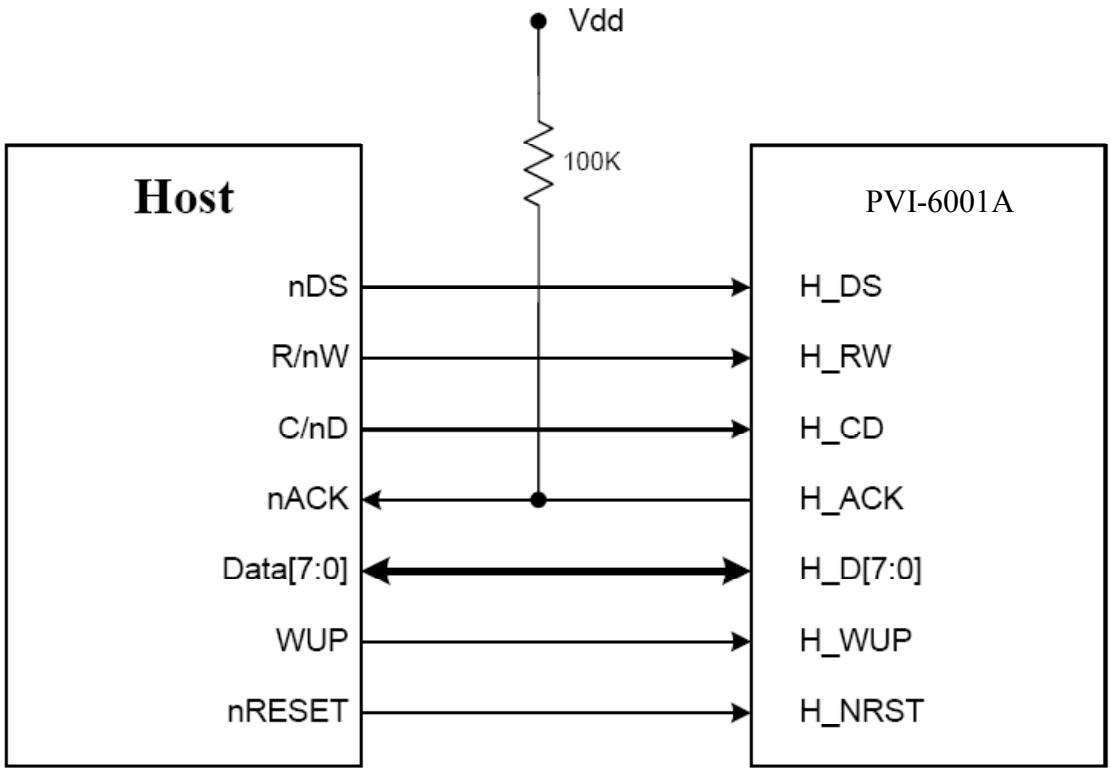


Figure 8.1 PVI-6001A host connection

8.2 Signal description
Individual terminals are as shown in table below.

Symbol name	Designation	Input/Output	Logic	Function
H_DS	Device select	Input	L	Data strobe
H_RW	Read/Write	Input	H: Read L: Write	Indicates the data bus Transfer direction.
H_D[7..0]	Data	3-state Input/Output		D: (7:MSB, 0:LSB)
H_CD	Command/Data	Input	H: Command, L: Data	Switching command or data
H_ACK	Acknowledge	3-state Output	L	Acknowledge
H_WUP	Wakeup	Input	H	Return from standby mode
H_NRST	Reset	Input	L	Reset(Asynchronous)

Table 8.1 Terminal designations and functions

8.2.1 H_DS
H_DS is a negative logic data strobe and is also the device enable signal. Data transfer is started, on the falling edge of the signal. The default value of the signal is logic “High”.

All data and control signals should be stable before the falling edge of H_DS. A positive setup time is required. The H_WUP and H_RW signals are only valid if the H_DS is “Low”.
When H_DS is “High” the H_ACK terminal is set to “Z” (tri-state).

If multiple display controllers are connected to a single host bus, the device selection is done with the H_DS signal. Each controller requires a unique H_DS connection. And only one controller can be addressed at a time. So it’s not allowed to have multiple H_DS signals “Low”.

Figure 8.2 shows the connection of H_DS and H_ACK when two controllers are used.

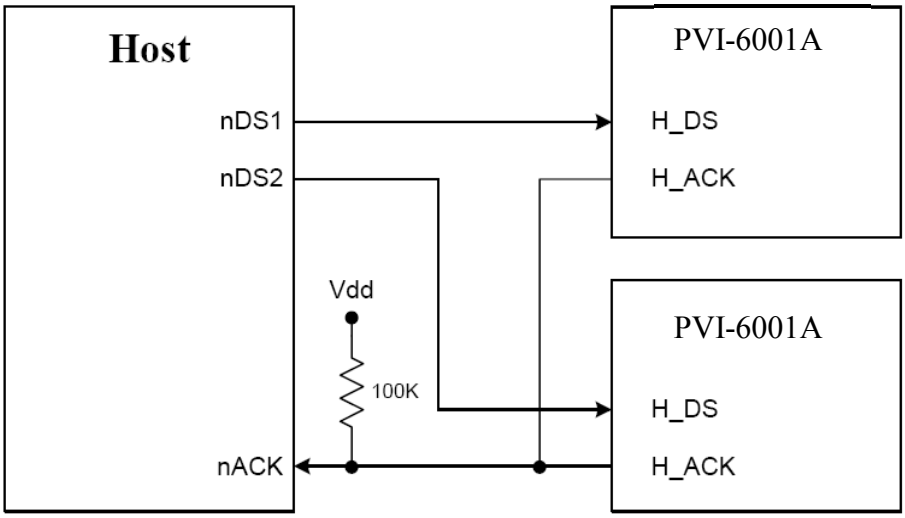


Figure 8.2 Connection of two controllers

8.2.2 H_RW
The input H_RW determines the data transfer direction. If the signal is “High” the controller is in the Read mode, and with “Low” in the Write mode.
The data bus direction is switched from input to output if H_RW and H_DS are logic “Low”

8.2.3 H_D[7:0]
Bi-directional 8 bits wide data bus. H_D0 is LSB and H_D7 is the MSB.

8.2.4 H_CD
H_CD indicates if the value on the data bus is intended as command or as data. When sending a command the H_CD needs to be logic “High” and for data, logic ”Low”.

When sending multiple data arguments the H_CD terminal should be “Low” at each falling edge of H_DS. If an intermediate command is send the loading of data is aborted.

When the H_RW signal is “High”, the signal H_CD is discarded.

8.2.5 H_ACK
The H_ACK signal is a negative logic acknowledge (similar indicator to BUSY).
H_ACK indicates the completion of data transfer.

As long as H_DS is “High”, H_ACK remains “Z” (tri-state). On the falling edge of H_DS, H_ACK is set to “High”. When the data transfer is completed, H_ACK is set to “Low”.
In the read sequence, H_ACK is set to “Low” if the data is valid. In the write sequence, H_ACK is set to “Low“ if the write is successfully.

Note that if multiple controllers are connected to a single host bus, the H_ACK signals from two or more individual controllers are wired-or connected as shown in Figure 8.2.

8.2.6 H_WUP
H_WUP is a signal required for returning from the standby mode. When H_WUP is “H” as positive logic, the controller in the standby mode switches into the sleep mode.
H_WUP is only valid if H_DS is “Low“.

For writing (commands or data) or reading sequences H_WUP should be set to “Low”.

Note that two or more H_DS terminals can never be switched to “Low” at the same time. So two or more controllers cannot be switched to sleep mode at the same time.

8.2.7 H_NRST
H_NRST is the host reset signal, which uses negative logic and is asynchronous.

8.3 Read and Write sequences
Read and Write sequences between the host and controllers are explained in detail. For the timing specification of the host bus see chapter 7.3 Timing host interface.

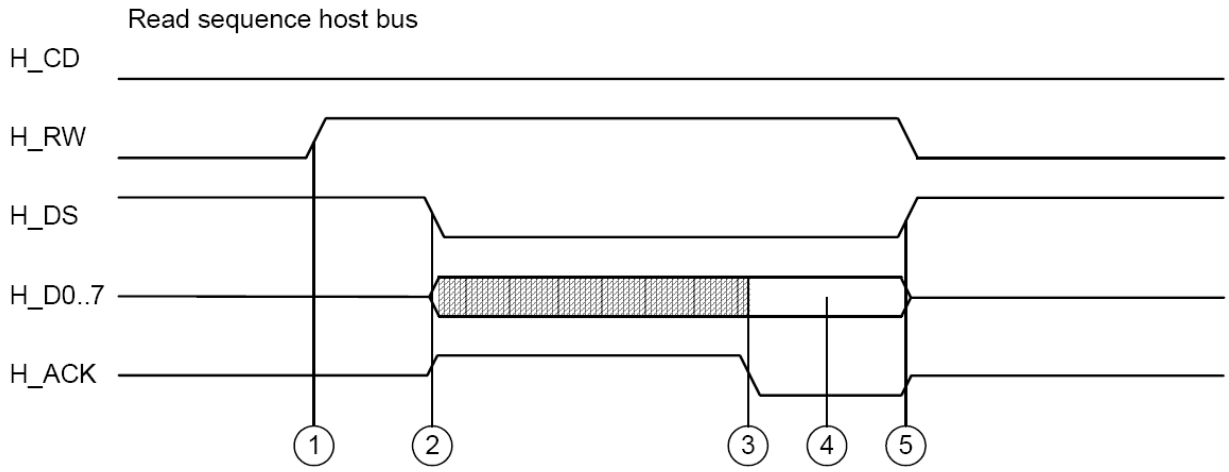


Figure 8.3 Explanation read sequence

Read sequence

1. The data bus is set to high impedance (“Z”) by the host and H_RW is set to “High”.
2. H_DS is set to “Low“. The controller makes H_ACK active “High” and the data bus direction is set to output.
3. The host waits until the data is valid and H_ACK is “Low”.
4. The host reads the data on the data bus.
5. The host sets H_DS back to “High”. The data bus and H_ACK are set to high impedance (“Z”).

8.3.1 WRITE SEQUENCE

Write sequence, a host writes commands or data to the controller.

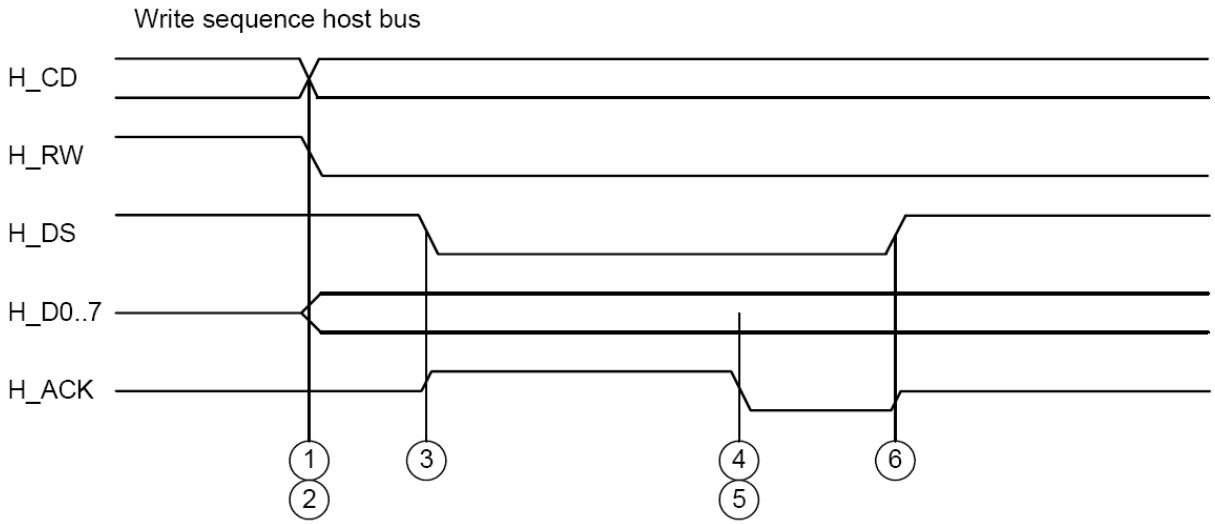


Figure 8.4 Explanation write sequence.

Write sequence.

1. H_RW is set to “Low”.
2. H_CD is set “High” in case of a command and “Low” in case of data. The data bus is set.
3. H_DS is set to “Low”. The controller makes H_ACK active “High”.
4. The controller latches the data bus value, and on completion switches H_ACK to “Low”.
5. The host waits until H_ACK is “Low”.
6. The host sets H_DS back to “High”. H_ACK is set to high impedance (“Z”).

8.3.2 H_ACK AND BUS ERROR

In the read or write sequence, a host needs to check if H_ACK is “L “ before finishing its sequence.

Please be aware that some operations take a very long time to complete. Like for instance display picture. The command itself will have a fast response however the next command will not be acknowledged until the previous command is completed.

If after a timeout of appropriate duration, (few seconds) there is still no acknowledge it might be a case of system failure. A reset can be issued with H_NRST to resolve the bus error.

8.3.3 READ PRECAUTIONS

The controller only returns data to the host after command has been issued that has a return value.

It is always possible to read data from the host bus, but the data is only valid if a previous command was issued that has a return value.

9. POWER MANAGEMENT FUNCTION

To make good use of the characteristics of E-ink display and to reduce its power consumption, the controller has the following power management modes.

9.1.1 NORMAL MODE

In the normal mode, a controller has all of its functions active and is capable of receiving any command. In this mode, a controller transfers data to the frame buffer and performs image drawing on the display.
The normal mode is also the default mode after reset. From sleep mode the “Normal mode ” command brings the controller into normal mode. The controller cannot go direct from standby mode to the normal mode. This has to be done via the sleep mode.

9.1.2 SLEEP MODE

The sleep mode is the mode to which the controller switches from the normal mode with the “Sleep mode” command. When the controller is in the sleep mode, only a limited part of the controller is active. In this mode, the circuit that drives the e-ink panel and the frame buffer is not operational. It also operates at the slow clock of only 70 Khz. The normal clock is shut down. Consequently the controller consumes less power in the sleep mode than in the normal mode.
The sleep mode is also entered from the standby mode with the “Wake Up” sequence.

In the sleep mode, the controller ignores those commands that cannot be processed, such as display. These commands can only be issued after the controller returns to the normal mode. Since the normal clock is stopped and needs to be restarted it requires some time to switch back to the normal mode.

9.1.3 STANDBY MODE

The standby mode is the mode to which the controller switches with the “Standby mode ” command. This mode stops all of the controller's functions. All clocks are shut down.

In the standby mode the controller consumes the least amount of power. The standby mode is useful when the controller is not used for a long time or the controller operations are stopped. The controller returns from the standby mode into the sleep mode with the “Wake Up” sequence.

In addition, it is impossible to switch from the standby mode to the normal mode directly. The controller shall always be switched to the sleep mode before switching to the normal mode.

Note:
It is mandatory to wait minimum 600 microseconds after the standby command before a wakeup sequence can be executed. After the standby command it is not allowed to issue a new command.

9.1.4 RETURN FROM STANDBY MODE

The controller returns from the standby mode to the sleep mode with the “Wake Up” sequence. The Wake Up sequence is activated by setting the H_WUP signal “High” before setting H_DS to “Low”.

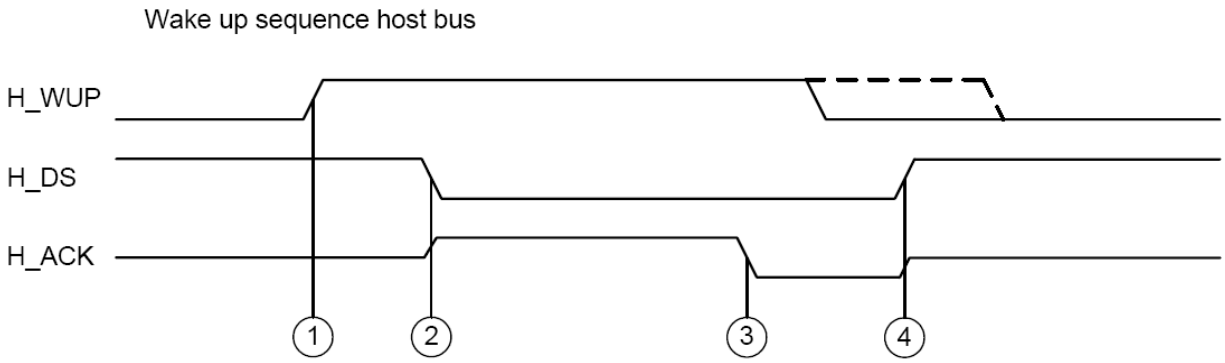


Figure 9.1 Wake Up sequence.

Wake Up sequence.

1. H_WUP is set to “High”.
2. H_DS is set to “Low“. The controller makes H_ACK active “High”.
3. The host waits until the mode switch is done and H_ACK is “Low”.
4. The host sets H_DS back to “High”. H_ACK is set to high impedance (“Z”).

Note:
It is allowed to set H_WUP “High” after H_ACK is “Low”. However this can also be done after the command is completed and H_DS is “High”.
H_WUP should be “Low” for all other operations than the Wake Up sequence.
It is mandatory to wait minimum 600 microseconds after the standby command before a wakeup sequence can be executed

9.1.5 TRANSITIONS FROM INDIVIDUAL MODES

The possible mode transitions are shown in Figure 9.2.

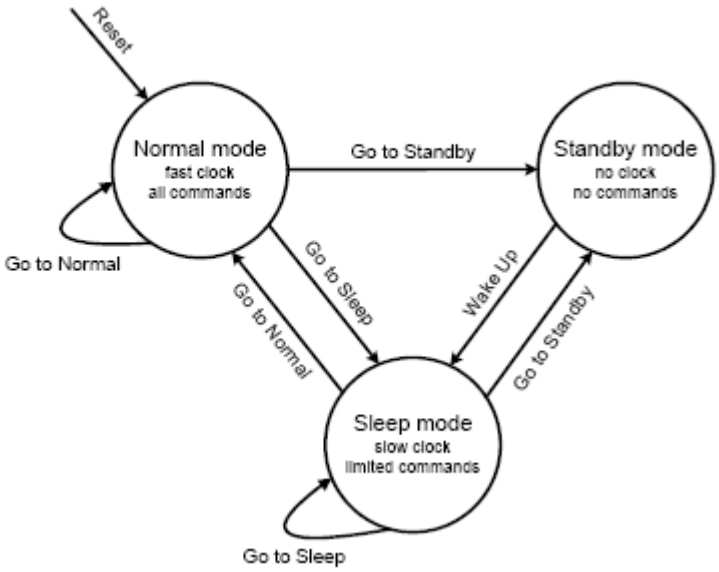


Figure 9.2 Mode transitions

10. COMMAND DESCRIPTION

This chapter provides information about the command set of the PVI-6001A Electrophoretic display controller and the statuses returned from the controller.

10.1 Command Lists

Table 10.1lists the commands covering drawing to the entire screen, Table 10.2 the commands covering drawing to part of the screen, Table 10.3 the commands directly controlling the controller, Table 10.4 the commands about power management, Table 10.5 the commands about controller setting, and Table 10.6 the commands about refreshment.

10.2 Command Details

Each command has a length of 1 byte and can be followed by one or more bytes of arguments. The arguments are data bytes. For commands H_CD is “High” for arguments (data) H_CD has to be set to “Low”.

Command name	Command	Mode	Argument	Return value	Operation
Load picture	0xA0	Normal	Image data	None	Transfers image data
Stop Loading	0xA1	Normal	None	None	Stops the transfer of image data
Display Picture	0xA2	Normal	None	None	Displays the image
Erase Display	0xA3	Normal	0,1,2,3	None	Erases the image
Init Display	0xA4	Normal	0,1	None	Initialize the display
Restore Picture	0xA5	Normal	None	None	Displaying previous Image

Table 10.1 Full-screen drawing commands

Command name	Command	Mode	Argument	Return value	Operation
Load Partial	0xB0	Normal	Coordinate and image data	None	Partially transfers image data
Display Partial Picture	0xB1	Normal	None	None	Displays the image

Table 10.2 Partial drawing commands

Command name	Command	Mode	Argument	Return value	Operation
Get Status	0xAA	Normal or Sleep	None	Status	Obtains the status
Version Number	0xE0	Normal	None	Version	Obtains the version of the controller
Display Size	0xE2	Normal or Sleep	None	Display size	Obtains the display size
Reset	0xEE	Normal or Sleep	None	None	Reset

Table 10.3 Control commands

Command name	Command	Mode	Argument	Return value	Operation
Normal mode	0xF0	Sleep	None	None	From the Sleep to Normal mode
Sleep mode	0xF1	Normal or Standby	None	None	To the Sleep mode
Standby mode	0xF2	Normal or Sleep	None	None	To the standby mode

Table 10.4 Power management commands

Command name	Command	Mode	Argument	Return value	Operation
Set Depth	0xF3	Normal	1Byte	None	Image data bits select
Orientation	0xF5	Normal	1Byte	None	Adjustable orientation With steps of 90°
Positive Picture	0xF7	Normal	None	None	Does not reverse the gradation.
Negative Picture	0xF8	Normal	None	None	Reverses the gradation
Write to Flash ROM	0x01	Normal	3 address bytes and 1 data byte	None	To write into Flash ROM
Read from Flash ROM	0x02	Normal	3 address bytes	1 data byte	To read from Flash ROM
Write Register	0x10	Normal	1 address byte and 1 data byte	None	To write into Register
Read Register	0x11	Normal	1 address byte	1 data byte	To read from Register
Read Temperature	0x21	Normal	None	Temperature	To read temperature

Table 10.5 Setting commands

Command name	Command	Mode	Argument	Return value	Operation
Auto Refresh	0xF9	Normal	None	None	Enables automatic Refresh.
Cancel Auto Refresh	0xFA	Normal	None	None	Disables automatic Refresh
Set Refresh Timer	0xFB	Normal	Timer set value	None	Set the refresh timer
Manual Refresh	0xFC	Normal	None	None	Refresh when next Image is displayed
Read refresh Timer	0xFD	Normal	None	Timer value	Obtains the refresh Timer value

Table 10.6 Refresh commands

10.2.1 LOAD PICTURE (0XA0)
The Load Picture command allows the host to write new image data of one screen to the controller. This data is stored in the external RAM and is used for the display update.
After the command byte is received, it is required to send the complete image data to the controller. The command is only valid in the normal mode.

The host continuously transfers 60 Kbytes of data for a binary image and 120 Kbytes of data for two bits grayscale. The command ends if the amount of data transferred is complete or if the Stop Load (0xA1) command is issued. It is recommended to send the Stop Load command always after finishing the execution of the Load Picture command.
For more information on the format of the image data see Chapter 13: Data format and Display waveform.

Note that the data being written does not appear immediately on the display. The picture appears on the display after the Display Picture command is executed.

10.2.2 STOP LOADING (0XA1)
The Stop Loading command allows the Load Picture and the Load Partial Picture commands to be aborted. It is recommended to use this command always after execution of the load commands. This is a safety measurement to return the controller into the idle state. The Stop Loading command is only valid if the controller is in the normal mode. The command has no arguments.

10.2.3 DISPLAY PICTURE (0XA2)
The Display Picture command displays the image data on the display.
The command is only valid in the normal mode. The command has no argument.
The Display Picture should not be executed if the controller does report that Load Picture has been aborted. This can be checked using the GetStatus command (see chapter 10.2.7).

10.2.4 ERASE DISPLAY (0XA3)
The Erase Display command allows the image on the display (and external memory) to be erased to all white, black, dark gray or light gray. The command allows high speed image erasing because no image data is sent.

This command is only valid in the normal mode. The command has one argument for the image content, 0x00 for black; 0x01 for white; 0x02 for dark gray and 0x03 for light gray. This argument is independent of the Positive or Negative Picture command.

10.2.5 INIT DISPLAY (0XA4)
The INIT command initiate the Electrophoretic display. It makes the display all white and insures that the data in the external memory is equal to the content on the display. The command is only valid in the normal mode.

An electrophoretic display has to be driven with the difference of the prior image and the new image. These images are stored in the external memory. The controller composes the display waveforms from the data stored in these external memories. If the memory is not equal to the display content, the controller cannot generate the correct image update.
The Init Display is used to generate a known content on the display and in the external memories (all white).

The command can be given in two situations.
1. Init after known all white display content. (Init argument= 0x00).
   The INIT command with argument 0 is to be used with known all white display content.
   Before powering down it is mandatory to make the display white. If the power is re-supplied the display content is known and the RAM content can be updated.
   So the init(0) only updates the external RAM. Pre-condition is that the complete display was in

the white state.
If images on an electrophoretic display are not updated for a long period there is some degradation of the image. To improve the quality of images on the display a refresh is executed on the displayed picture after the init (0). See also the refresh command.

2. Init with other or unknown display content. (Init argument= 0x01).
The INIT command with argument 1 is to be used when power re-supplying after accidentally power removing. In this case the controller has lost both the screen image and the image data in the frame buffers. This command is also useful for first time use of the display system as he screen image is undefined and also the image data in the frame buffers is undefined.

Note:
It is not necessary to perform an init after a reset. This is only required if the external SRAM are powered down.

10.2.6 RESTORE PICTURE (0XA5)
The Restore Picture command allows displaying the previous displayed image. Repeating this command allows two images displaying alternately. This command is valid only when the controller is in the normal mode. This command has no argument.
On the execution of this command the contents of the external memories are kept unchanged, so this makes immediate displaying possible without any new data sending for e.g. icon on/off flashing or to recover the last image.

10.2.7 GET STATUS (0XAA)
The Get Status command returns one byte data of the actual status of the controller.
The command is valid in the normal and sleep mode. The command has no argument.
For details see 12.

Bit	Item	Description
0	Operation mode status	0:Normal mode, 1: Sleep mode
2,1	Screen status	00: No Picture 01: Picture is loaded 10: Picture has been displayed 11: Loading of Picture has been aborted
3	Auto Refresh status	0:Autorefresh = off; 1:Autorefresh = on
4	Display data mode	0: 1bit Black/White; 1: 2bits Gray-scale
5	Reserved	Reserved
6	Reserved	Reserved
7	Reserved	Reserved

Table 10.7 Detail of Status bits.

10.2.8 LOAD PARTIAL PICTURE (0XB0)
The Load Partial Picture command allows the use of sub-picture(s) in a picture. It can be particular useful for displaying text b0xes. Multiple partial pictures can be displayed, but after each load partial display picture, a display picture command is required before the next Load Partial Picture Command can be issued. The command is only valid in the normal mode.

The partial picture area is denoted by a rectangle with a top left point (x_1, y_1) and a bottom right point (x_2, y_2), as shown in Figure 10.1. The pointers coordinates are the first 8 arguments followed by the

display data. Each coordinates are 4 bytes (2 bytes for x, and 2 bytes for y). The image data has the same format as the load display command.

The coordinates are only valid numbers in steps of 4 pixels. As well for horizontally and vertically coordinates. All coordinates (x_1, y_1, x_2, y_2) have to be multiples of 4. Starting with 0.
So 0, 3, 7…595, 599…791 795, 799 are all valid coordinates. Whereas 1, 4 and 800 are **invalid** coordinates. This implies that the partial image area and size are all multiples of 4 pixels.

The command ends if the correct quantity of sent data or if the Stop Loading command is issued. After the end of data transfer, the Display Partial Picture command shall be used to display the image on the display.

Note:
Since it requires some time for address decoding the, data transfer may take some extra time. And the data transfer rate can be lower than with the load picture command.

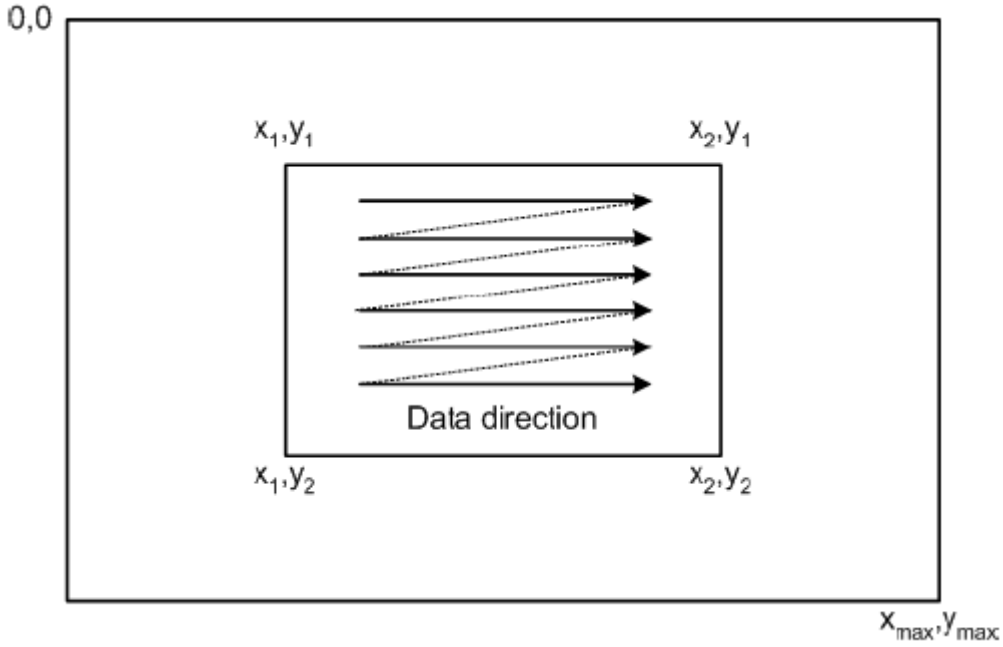


Figure 10.1 Coordinate designation for partial drawing

10.2.9 DISPLAY PARTIAL PICTURE (0XB1)
The Display Partial Picture Command is identical with the Display Picture Command. See chapter 10.2.3

10.2.10 VERSION NUMBER (0XE0)
The Version Number command returns the version number of the PVI-6001A. The command is valid in the normal and the sleep mode. The command has no argument and one return byte. The version number is a hexadecimal number.

10.2.11 DISPLAY SIZE (0XE2)
The Display Size returns the resolution of the display and the maximum bits grayscale that can be displayed. The command is valid in the normal and the sleep mode. The command has no argument and one return byte.

Returned byte is 0x22. This indicates a display resolution of 800x600 pixels and 4 bits grayscale level. Other values are reserved for future developments.

10.2.12 RESET (0XEE)
The Reset command is a soft reset of the controller. The reset is a complete reset equivalent to a hardware reset. The command is valid in the normal mode or sleep mode. The command has no argument.

Notes:
This command deviates somewhat of normal commands. The Reset Command is not executed when the command is acknowledged, but after the write sequence has completed. (H_DS is returned to “High”). This is done so the acknowledge signal is not cancelled by the reset and the normal writing sequence can be used. Only the reset command has this behavior all other commands are executed if the command is acknowledged.

It is recommended to wait for a period of 20 microseconds after the reset command is completed before a new command is issued.

10.2.13 NORMAL MODE (0XF0)
The Normal Mode command causes the controller to return from the sleep mode to the normal mode. The command is valid only when the controller is in the sleep mode. The command has no argument. For more information on the normal mode see Chapter 9.1.1.

10.2.14 SLEEP MODE (0XF1)
The Sleep Mode command causes the controller to switch to the sleep mode. The sleep mode stops the primary 33Mhz clock and individual blocks. This mode is very useful for switching to a low power mode while leaving the controller operational. Since the controller is running on a slower clock speed (70Khz) the respond time is larger.

The controller can switch from the sleep mode to either the normal mode or the standby mode freely. For more information on the sleep mode see Chapter 9.1.2.

The command is valid in the normal mode or sleep mode. The command has no argument.

10.2.15 STANDBY MODE (0XF2)
The Standby Mode command causes the controller to switch to the standby mode. The command is valid in the normal and the sleep mode. The command has no argument.

The standby mode is used for stopping the operation of the controller. It stops all of its functions including communication with the host and shuts all clocks down. The controller returns from the standby mode with the Wake Up sequence.

Note:
It is mandatory to wait minimum 600 microseconds after the standby command before a wakeup sequence can be executed. After the standby command it is not allowed to issue a new command.

10.2.16 SET DEPTH (0XF3)
The Set Depth command sets the data depth (number of bits) for each pixel. The command is valid only when the controller is in the normal mode. The command has one byte argument, see Table 10.8. This controller only supports the binary and 2 bits grayscale mode.

This mode results only in a change for the data format to besent.

Since the image data is 800x600 pixels, the total transfer data is 60kB in binary mode or 120kB in 4 levels grayscale mode. Thus the data transfer time in the grayscale mode is almost twice of the binary mode.

Note that if an undefined size of Set Depth is sent, this will result in an incorrect image update.

Argument	Data depth (data bit number/pixel)
0x00	1 bit/p (Black/White)
0x01	Reserved
0x02	2 bits/p (4 level grayscale)
others	Reserved

Table 10.8 Argument of Set Depth commands

The Set Depth command has no direct effect on the grayscale level of the displayed image, or on the used waveform. The displayed grayscale level is explained in detail in Chapter 13

10.2.17 ORIENTATION (0XF5)

The Orientation command allows the display orientation to be rotated with steps of 90 degrees clockwise. The command is only valid in the normal mode. The command has an argument as in table 3.11. With this command it is possible to change the orientation of the display. It is not possible to rotate pictures on the display. Only the orientation of the image can be changed.
This command has no direct effect on the current image on the display. It only has an effect on new data and must therefore be issued before a corresponding Load command.

Argument	Orientation
0x00	Landscape = no rotation
0x01	Portrait = 90 degrees rotation
0x02	Landscape mirrored = 180 degrees rotation
0x03	Portrait mirrored = 270 degrees rotation

Table 10.9 Argument of Rotate commands

Fig.3.2 indicates the rotation of the orientation defined by the Orientation command. The default mode is Portrait. (90 degrees mode).

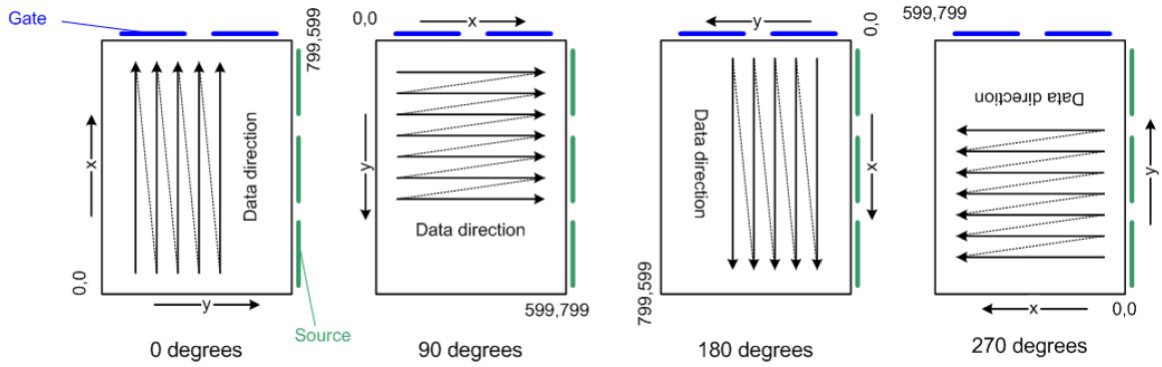


Figure 10.2 Display area according to rotate command

10.2.18 POSITIVE PICTURE (0XF7)

The Positive Picture command allows the gradation to appear un-reversed. The command is only valid in the normal mode. Default mode of the controller is the un-reversed gradation. The command has no argument.

For the binary mode, for example, pixel data 0 turns black while pixel data 1 turns white. Immediately after resetting, the controller is in this mode.

The command has no direct effect on the current image. It only has an effect on new data and must therefore be issued before a corresponding load command.

10.2.19 NEGATIVE PICTURE (0XF8)
The Negative Picture command allows the gradation to appear reversed. The command is only valid in the normal mode. The command has no argument.

For the binary mode, for example, pixel data 0 turns white while pixel data 1 turns black.
The command has no direct effect on the current image. It only has an effect on new data and must therefore be issued before a corresponding load command.

10.2.20 WRITE TO FLASH ROM (0X01)
The controller uses an external Flash ROM memory as Look-Up-Table. With the write to flash Rom command it is possible to writeto the external Flash ROM and can be used to program the flash memory. For more information see application note on programming a flash memory.

The command is only valid in the normal mode and has four arguments. (3 address bytes and 1 data byte)

10.2.21 READ FROM FLASH ROM (0X02)
The controller uses an external Flash ROM memory as Look-Up-Table. With the Read from Flash Rom command it is possible to read from the external Flash ROM and can be used to poll the status of the flash memory, debugging and to check the connections of the Flash Rom. For more information see application note on programming a flash memory.

The command is only valid in the normal mode and has three arguments. (3 address bytes) and has one return value (data byte)

10.2.22 WRITE REGISTER (0X10)
The controller uses internal registers for optional settings. The write register command can write and change these settings. For more information on the internal settings see Chapter 11.

The command is only valid in the normal mode and uses two arguments (1 address bytes and 1 data byte. The command has no return value.

10.2.23 READ REGISTER (0X11)
The controller uses internal registers for optional settings. The read register command can read out the actual settings. For more information on the internal settings see Chapter 11.

The command is only valid in the normal mode and uses 1 argument (1 address bytes) and has one return value (data byte).

10.2.24 READ TEMPERATURE (0X21)
The controller uses a digital temperature sensor to determine the ambient temperature. This is used to compensate the temperature behavior of the display. The temperature is determined during a display sequence.

With the read temperature command it is possible to get the read out from the temperature sensor. The command is only valid in the normal mode and has no arguments. The return value is one signed byte.
Note that the temperature is not updated with a read temperature command and is not the actual temperature but the stored value measured in the last display sequence. To update the temperate a display command has to be executed first.

10.2.25 AUTO REFRESH (0XF9)

If images on an electrophoretic display are not updated for a long period there is some degradation of the image. This also has an impact on the pictures displayed afterwards.
To improve the quality of images on the display it is possible to apply a touch-up waveform before a new image is displayed. This is called a refresh.
The refresh is executed on the next display update and sees to it that the next pictures are displayed with an improved quality. With the Auto refresh command the refresh is done on an adjustable period.
The refresh is also executed after a return from standby mode.

The command is only valid in the normal mode and has no arguments.

10.2.26 CANCEL AUTO REFRESH (0XFA)

The cancel auto refresh disables the auto refresh.
The command is only valid in the normal mode and has no arguments.

With the cancel auto refresh, the count down of the refresh timer is disabled. After enabling the counter via the auto refresh command the counter will count down again from the value it was stopped. The use of this command may have a negative impact on the optical performance of the display. Its use should be restricted to short periods when a refresh operation cannot be tolerated.

Note:
If the refresh is cancelled for a long period it is advised to execute a manual refresh to ensure optimal image quality

10.2.27 SET REFRESH TIMER (0XFB)

The set refresh timer sets the interval timer used in the auto refresh.
The command is only valid in the normal mode and has one argument (timer value).

The timer setting operation is done at every 6-seconds step. The actual time can be obtained by multiplying the value by 6. Therefore, the maximum value for the timer is appr0ximately 25 minutes.
The default value is 0x64 corresponding to 10 minutes.

10.2.28 MANUAL REFRESH (0XFC)

The manual refresh causes the refresh time to be set to zero such that at the next display command a refresh is executed. The command is only valid in the normal mode and has no arguments.

10.2.29 READ REFRESH TIMER (0XFD)

The Read Refresh Timer returns the current value of the refresh timer and shows how much time is left before the next refresh is executed.
The command is only valid in the normal mode and has no arguments. The returned value is one byte. The actual time is the retrieved value multiplied by 6 in seconds.

11. REGISTER DETAILS

The controller uses internal registers for optional settings. With the settings several options can be chosen.

11.1 Common PWM

The controller has a PWM output COM_PWM that can be set between 0 and 100% duty cycle. Default value = 0xFF (100%).

Name	Address	Value	Default
COMMON_PWM	0x11	Duty cycle [0..100%]	0xFF

11.2 Border

This register can be used to test the border functionality. The register is a mirror of the border pixel prior and current state. The register is updated every display update. The register is restricted for testing of the PVI-6001A display controller only and should not be used in final application.

Name	Address	Value
Border	0x12	[x x P_1 P_0 x x C_1 C_0]

P1 = MSB prior state

P0 = LSB prior state

C1 = MSB current

C0 = LSB current state

11.3 Look up table.

The controller can handle multiple look up table. With this register a selection between look-up-tables can be made. Default value is 0. The controller can handle maximum 16 LUT's. [0..15]. The register is restricted for testing of the PVI-6001A display controller only and should not be used in final application.

Name	Address	Value	Default
LUT select	0x13	0..15 decimal	0x00

11.4 SRAM

The controller uses external SRAM memories to store the images. With these registers it is possible to set and read out these registers. The registers are mainly used for debugging and for testing the connection between PVI-6001A and the SRAM.

To write and read, set the correct address and data and write to the SRAM control register. The address is incremented automatic after each operation (read or write).

Name	Address	Value	Default
Address Byte 2	0x14	bit 23-16 of the address bus.	0x00
Address Byte 1	0x15	bit 15-8 of the address bus.	0x00
Address Byte 0	0x16	bit 7-0 of the address bus.	0x00
SRAM ctrl	0x17	Bit1 = write, bit0 = read	0x00
Data byte3	0x1A	SRAM data bits 31-24	0x00
Data byte2	0x1B	SRAM data bits 23-16	0x00
Data byte1	0x1C	SRAM data bits 15-8	0x00
Date byte0	0x1D	SRAM data bits 7-0	0x00

11.5 Source Data

This register can be used to set fixed data to the source driver. To switch from normal data to the data from the register bit3 of the auxiliary register has to be set to “1”. The register is restricted for testing of the PVI-6001A display controller only and should not be used in final application.

Name	Address	Value	Default
Source data	0x18	Data to source driver.(enable auxiliary registers)	0x00

11.6 Auxiliary. (demo mode)

This register is used to test parts of the ASIC and enables internal functions.
The controller can display images stored in the Flash memory. This demo mode is controller via bit 1 and bit 0 of the register. The register is restricted for testing of the PVI-6001A display controller only and should not be used in final application.

Name	Address	Value	Default
Demo mode	0x1F	X X X B S G D1 D0	0x00

B = Booster soft start on.

S = Enable source data from register

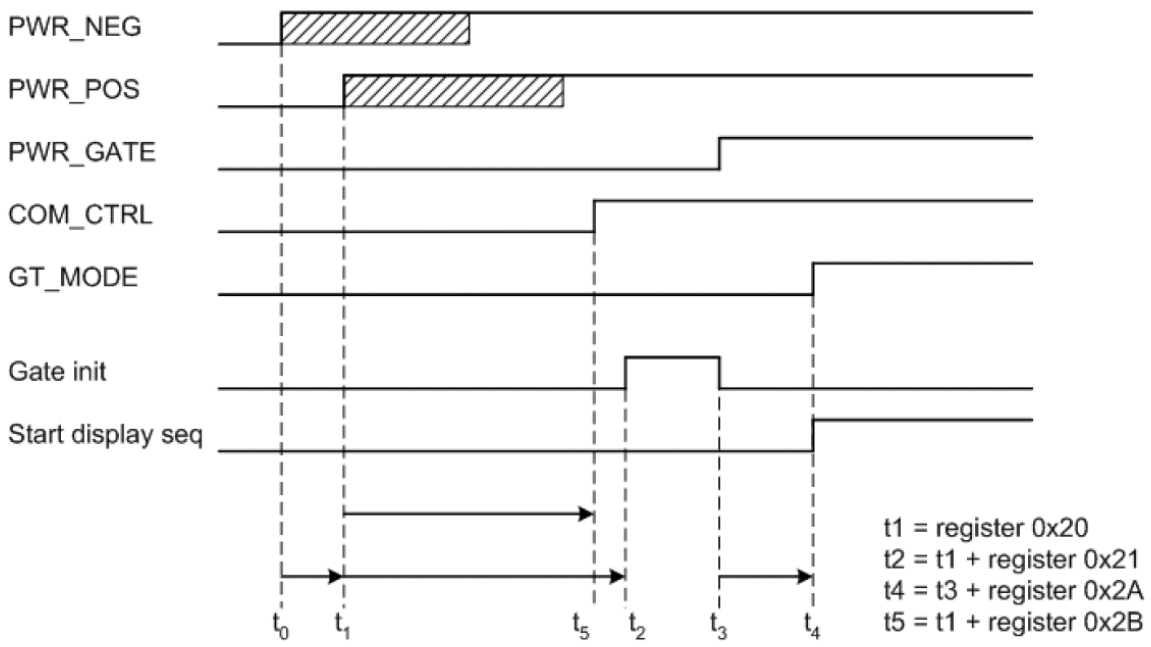
G = Disable gate driver

D1 = Start demo mode.

D0 = Stop demo mode.

11.7 Power supply.

The PVI-6001A controller has a number of pins that can be used to control external power supplies for the display on and off.



The PWR_NEG and PWR_POS pin also has a soft-start feature. These outputs can be turned on pulsed for a short period. This can be used to implement a softstart.

Name	Address	Value	Default
t1 delay	0x20	Decimal value x 0.49 milliseconds	0x00
t2 delay	0x21	Decimal value x 0.49 milliseconds	0x8E(70 msec)
t4 delay	0x2A	Decimal value x 0.49 milliseconds	0x0A(4.9 msec)
t5 delay	0x2B	Decimal value x 0.49 milliseconds	0x70(55 msec)
Off delay	0x22	Turn off delay = decimal value x 0.5 sec	0x00
Soft time neg	0x23	Decimal value x 0.49 milliseconds	0x00
Soft period neg	0x24	Decimal value x 240 nanoseconds	0xA6(40 μ sec)
Soft length neg	0x25	Decimal value x 240 nanoseconds	0x7D(30 μ sec)
Soft time pos	0X26	Decimal value x 0.49 milliseconds	0x00
Soft period pos	0X27	Decimal value x 240 nanoseconds	0xA6(40 μ sec)
Soft length pos	0x28	Decimal value x 240 nanoseconds	0x7D(30 μ sec)

11.8 Refresh timer.
The refresh timer is made from the slow clock. If the slow clock is not equal to 70 kHz it is possible to calibrate the refresh timer with this register.

The refresh time interval should be 6 seconds. The value can be calculated by clock period x register value x 4096.

Name	Address	Value	Default
Calibrate refresh	0x29	Decimal value x slow clock period x 4096	0x33

11.9 Temperature sensor.
The controller uses a digital temperature sensor to determine the ambient temperature. The temperature setting can be overruled by a register value.
To overrule the temperature setting a register has to be set to switch between data of the temperature setting or the register.
The register is restricted for testing of the PVI-6001A display controller only and should not be used in final application.

Note:
The temperature sensor should always be connected to the I2C bus to ensure correct behavior of the I2C bus.

Name	Address	Value	Default
Switch temp	0x40	bit 0 switches enables internal register	0x00
Temp data	0x41	Temperature data signed	0x18

12. STATUS DETAIL

The Get Status command allows the controller to return one-byte status information to the host. Individual statuses are allocated to individual bytes.

Bit 0: Operation mode status

The Bit0 shows the power management status for the controller. Numeral 1 represents the sleep mode, and numeral 0 the normal mode.

Bit 1-2: Screen status

The Bit 1-2 shows the screen status. Two bits are allocated. Individual combinations of these two bits are shown in Table 3.12.

Bit2	Bit1	Operation
0	0	No picture is drawn to the screen.
0	1	Picture is loaded
1	0	Picture has been displayed
1	1	Loading of Picture has been aborted

Table 12.1 Screen status

Bit 3: Auto Refresh status

The Bit3 shows the automatic refresh status. Numeral 1 indicates that the auto refresh operation is valid and numeral 0 indicates that the operation is invalid.

Bit 4 Display data mode

The Bit4 shows that the image data mode is 2 bits or 1 bit. Numeral 1 represents 1 bits input data and numeral 0 represents 1bit data mode.

Bit 5 – Bit7: Reserved

The Bit5-Bit7 are reserved. Numeral 0 is always allocated.

13. DATA FORMAT AND DISPLAY WAVEFORM

13.1 Binary Display Mode

In the binary display mode, one pixel is represented by one bit. Therefore one byte has 8 pixels of data.

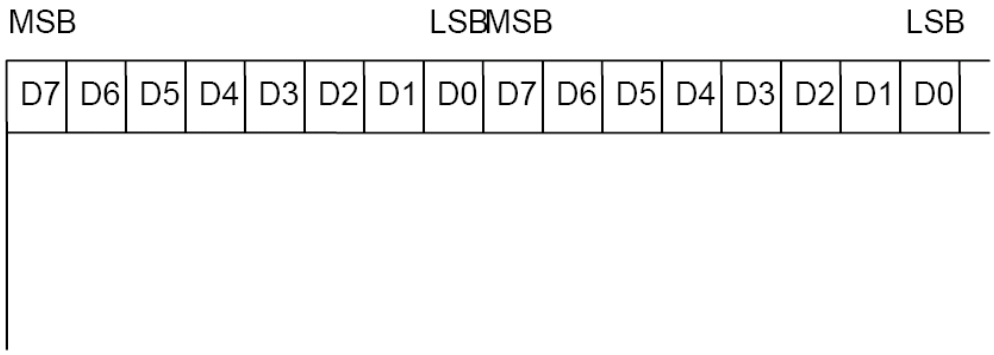


Figure 13.1 Data format binary mode

Figure 13.1 shows a binary display mode data format. Data is arranged such that it starts with the top left pixel as the MSB (D7) and the next pixel is regarded as D6. The 8th pixel serves as the LSB (D0). The 8th pixel is followed by the next one byte of data, which is arranged in a similar manner. This mode requires 60 Kbytes of data for a complete image.

13.2 Four Levels Grayscale Display Mode

In the 4 levels grayscale display mode, one pixel is represented by two bits. Therefore one byte has 4 pixels of data.
Figure 13.2 shows a 4 levels grayscale display mode data format. Data is arranged such that it starts with the top left pixel on the most significant bits D7 and D6. The 4th pixel are the least significant bits D1 and D0. The 4th pixel is followed by the next one byte of data, which is arranged in a similar manner. This mode requires 120 KBytes of data for a complete image.

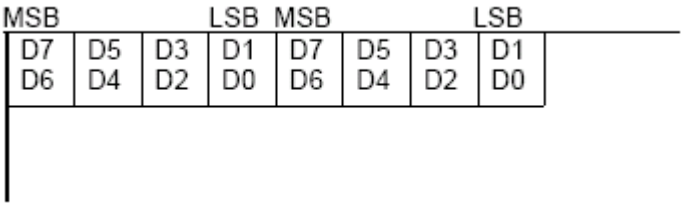


Figure 13.2 Levels grayscale display mode data format

D7/D5/D3/D1	D6/D4/D2/D0	Gradation
0	0	Black
0	1	Dark Gray
1	0	Light Gray
1	1	White

Table 13.1 Data – 4Levels Gray scale relationship

13.3 Display Update Operations – Monochrome vs. Grayscale

The electrophoretic display has two different update modes, depending upon the bit depth of the images to be displayed. For updating monochrome (black and white) pixels only, the display controller adopts a fast waveform with direct transitions between black and white. This allows for so-called general image flow (GIF) updates, in which images flow smoothly from one to the next.

For updating pixels to or from one of the intermediate gray states, the display controller adopts a slower waveform, designed to give high-quality grayscale images.

To determine which of these update sequences to use for a given display update, the controller compares the new and previous image data in memory. If any of the pixels that are changing are going to or from an intermediate gray state, then the controller uses the slower grayscale update for the entire image. Instead, if all of the pixels that are changing are only transitioning from black -> white or white -> black, then the faster monochrome update sequence is used.

It should be emphasized that only the pixel values of the changing pixels will determine the update sequence to be used. Specifically, the format of the data (1-bit vs. 2-bit) that is sent to the display will have no effect on the update sequence. Also, the gray levels of any unchanged pixels on the display do not affect the update choice.

This update logic can be used by the host system to initiate a rapid sequence of monochrome updates, by ensuring that all pixels being updated are black and white only. For example, to type text over a grayscale bitmap, the controller could first blank a portion of the display to white or black, and then display the typed characters in that region using a 1-bit depth font.

14. THE DEFAULT VALUE AFTER RESET

The controller has reset possibilities.
- POR. Which is usually done at power on to ensure correct power up of the device.
- Hardware reset with the H_NRST input.
- And the third one is the software reset by the Reset command.

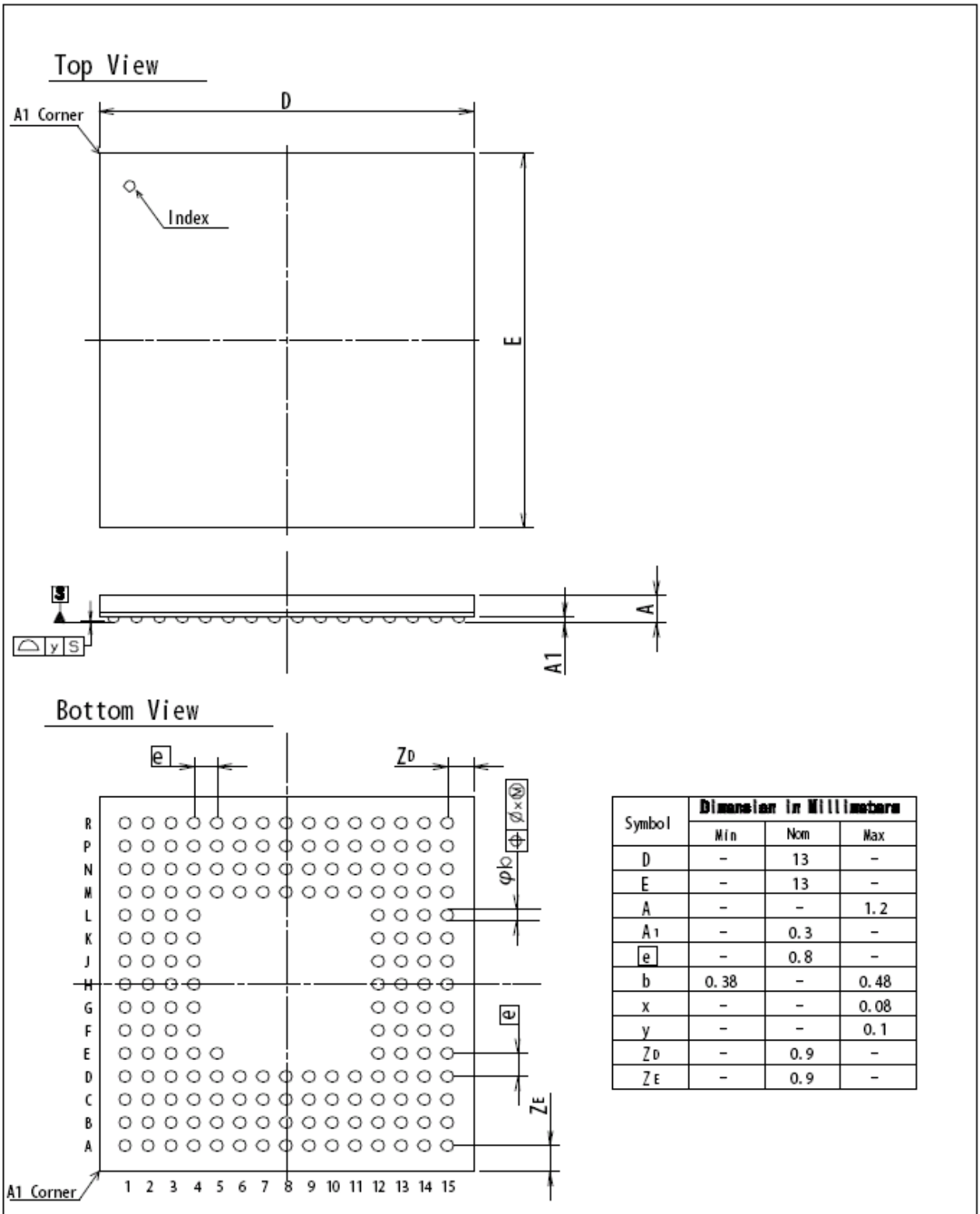
All these resets perform the same operation.

Please be aware that if the external memories are powered down the content of the memories is not guaranteed and an init procedure should be performed. The controller saves its pointer in the SRAM so it is not necessary to perform an init after a reset. Only if the external SRAM are powered down.

Item	Initial Condition
Power management mode	Normal mode
Set Depth	Binary mode
Rotation	90 degrees mode(portrait)
Image Inversion	Positive mode
Auto refreshment	Auto Refresh mode
Refresh Timer	10 minutes

Table 14.1 Default after Reset

APPENDIX A: PACKAGE INFORMATION



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	13	-
E	-	13	-
A	-	-	1.2
A1	-	0.3	-
e	-	0.8	-
b	0.38	-	0.48
x	-	-	0.08
y	-	-	0.1
ZD	-	0.9	-
ZE	-	0.9	-

1 = 1mm

REV.	DATE	DRAW	CHECKED	APPROVED	
1.0	2006.01.23	K. MIKAMI	M. SONE	T. OTSUKI	—
					CORRECTION ARTICLE

TITLE: P-TFBGA-177-1313-0.80(PFBGA13U-177)

CAD FILE: —

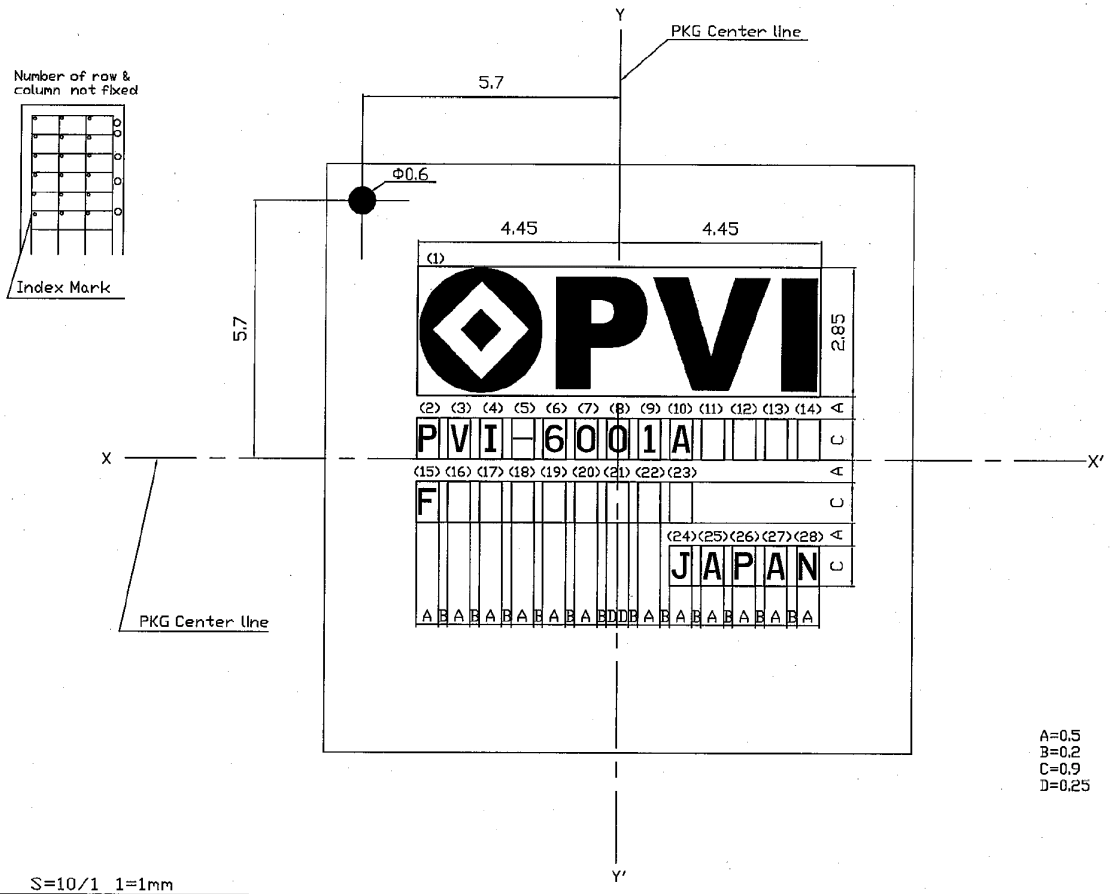
DWG No. 4900-0398

SCALE: Free SHEET 1 of 1

SEIKO EPSON CORP.

MARKING SPEC.

別紙 1



EXPLANATION OF MARK[:FIXED(固定)] S=10/1 1=1mm

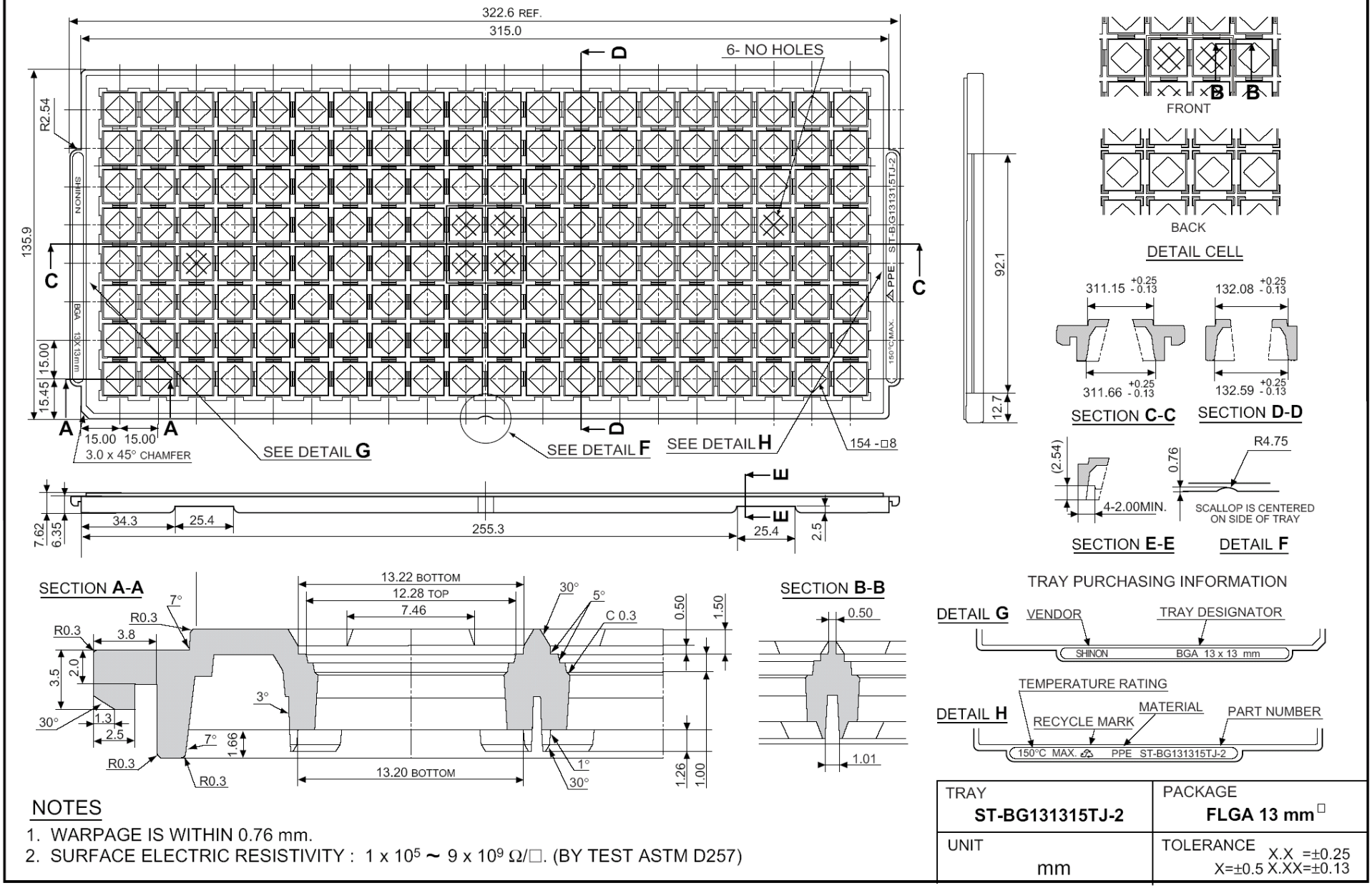
ITEM (項目)	No.	NOTE. (備考)
*CUSTOMER MARK(ユーザーマーク)	(1)	REFER TO LOGO TYPE FIXED(指定ロゴ使用)
*NAME OF GOODS (機種名)	(2)~(14)	(11)~(14) BLANK
*「JAPAN」	(24)~(28)	
CONTROL CODE (管理コード)	(15)~(23)	
*「F」	(15)	
YEAR OF MANUFACTURE (製造年)	(16)~(17)	LAST TWO NUMBER OF A.D. (西暦下2桁)
WEEK OF MANUFACTURE (製造週)	(18)~(19)	CALENDAR WEEK OF THE YEAR (1月1日を含む週01より通番)
W/F LOT No.	(20)~(23)	e.g. 0106 → 0106 IC生産管理部門より指定 1254 → 1254 される4桁のウェハロットNo. S352 → S352

PFBGA13UX 用

REV.	DATE	DESC.	APPD	CHKD.	DRAW	CUSTOM	CONTENTS
			Masuya 3/15	Masuya 3/15			

NAME	PVI-6001A (S1X56243B00A000)
PACKAGE TYPE	PFBGA13UX-177PIN
DEVICE CODE	
ASSEMBLY SPEC.	No.
TEMPLATE.	No. FPB177Y0063

SEIKO EPSON CORP. 0190-0117*付表-5-2*REV.5



NOTES

1. WARPAGE IS WITHIN 0.76 mm.
2. SURFACE ELECTRIC RESISTIVITY : 1 x 10^5 ~ 9 x 10^9 Ω/□. (BY TEST ASTM D257)

TRAY **ST-BG131315TJ-2**	PACKAGE **FLGA 13 mm□**
UNIT mm	TOLERANCE X.X =±0.25 X=±0.5 X.XX=±0.13

APPENDIX B: BLOCK DIAGRAM REFERENCE DESIGN