



Genesys Logic, Inc.

GL811S

**USB 2.0 to ATA/ATAPI
Bridge Controller**

**Datasheet
Revision 1.02
Apr. 13, 2007**



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Office:

Genesys Logic, Inc.

12F, No. 205, Sec. 3, Beishin Rd., Shindian City,

Taipei, Taiwan

Tel: (886-2) 8913-1888

Fax: (886-2) 6629-6168

<http://www.genesyslogic.com>



Revision History

| Revision | Date | Description |
|----------|------------|--|
| 1.00 | 03/09/2006 | First release |
| 1.01 | 05/25/2006 | Modify GL811S 48 Pin TQFP Package, Figure 7.2, p.37 |
| 1.02 | 04/13/2007 | Remove 48Pin TQFP Pinout, p.9 and 48Pin TQFP Dimension, p.35 |



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CHAPTER 1 GENERAL DESCRIPTION

The GL811S is a highly-compatible, low cost USB 2.0 to ATA / ATAPI bridge controller, which integrates Genesys Logic own design high speed UTMI (USB 2.0 Transceiver Macrocell Interface) transceiver.

As a one-chip solution which complies with Universal Serial Bus specification rev. 2.0 and ATA / ATAPI-6 specification rev 1.0, the GL811S can support various kinds of ATA / ATAPI device. There are totally 4 endpoints in the GL811S controller, Control (0), Bulk In (1), Bulk Out (2), and Interrupt (3). By complies with the USB Storage Class specification ver.1.0 (Bulk only protocol), the GL811S can support not only plug and play but also Windows XP/ 2000/ ME default driver.

The GL811S uses 12MHz crystal and slew-rate controlled pads to reduce the EMI issue. With 48-pin LQFP (7mmX7mm) package, the GL811S is the best cost/ performance solution to fit different situations in the USB 2.0 high speed storage class applications such as Hard Disk, CD-ROM, CD-R / RW and DVD-ROM.



CHAPTER 2 FEATURES

- Complies with Universal Serial Bus specification rev. 2.0.
- Complies with ATA/ATAPI-6 specification rev 1.0.
- Complies with USB Storage Class specification ver.1.0. (Bulk only protocol)
- Operating system supported: Win XP / 2000 / Me / 98 / 98SE; Mac OS 9.X / 10.X.
- Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) transceiver and Serial Interface Engine (SIE).
- Support 4 endpoints: Control (0) / Bulk Read (1) / Bulk Write (2) / Interrupt (3).
- 64 / 512 bytes Data Payload for full / high speed Bulk Endpoint.
- Support 16-bit Multiword DMA mode and Ultra DMA mode interface (Ultra 33 / 66).
- Embedded Turbo 8051.
- ROM size: 12k words; RAM size: 1280 bytes. (Bulk Buffer: 512 words, MC RAM: 256 bytes)
- Supports Power Down mode and USB suspend indicator.
- Supports USB 2.0 TEST mode features.
- Supports 4 GPIOs for programmable AP (48 pin package).
- Supports 8 GPIOs for programmable AP (64 pin package).
- Supports device power control for power on/off when running suspend mode.
- Supports 32 bit and 48 bit LBA hard disk.
- Provides LED indicator for Full Speed and High Speed (only for 64 pin package).
- Using 12 MHz external clock to provide better EMI.
- 3.3V I/Os (5V tolerant) 5V tolerance pad for IDE interface.
- Operates at 5V voltage (built-in 5V to 3.3V & 3.3V to 1.8V regulator)
- Supports Wakeup ability.
- Available in 48-pin/64-pin LQFP package types.
- Provides SPI interface (only for 64 pin package).
- Provides UART interface (only for 64 pin package).

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

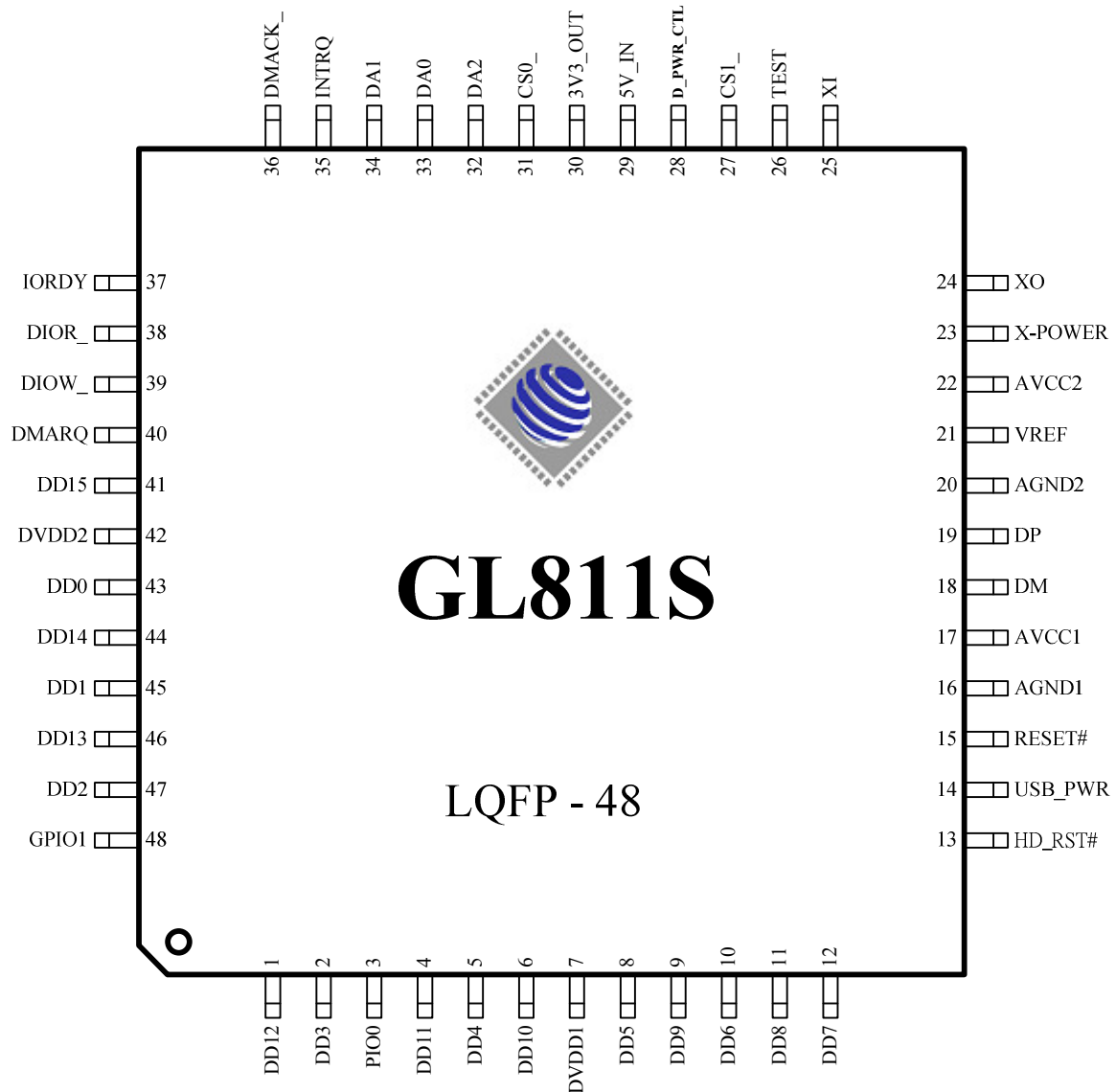


Figure 3.1 - 48 Pin LQFP Pinout Diagram

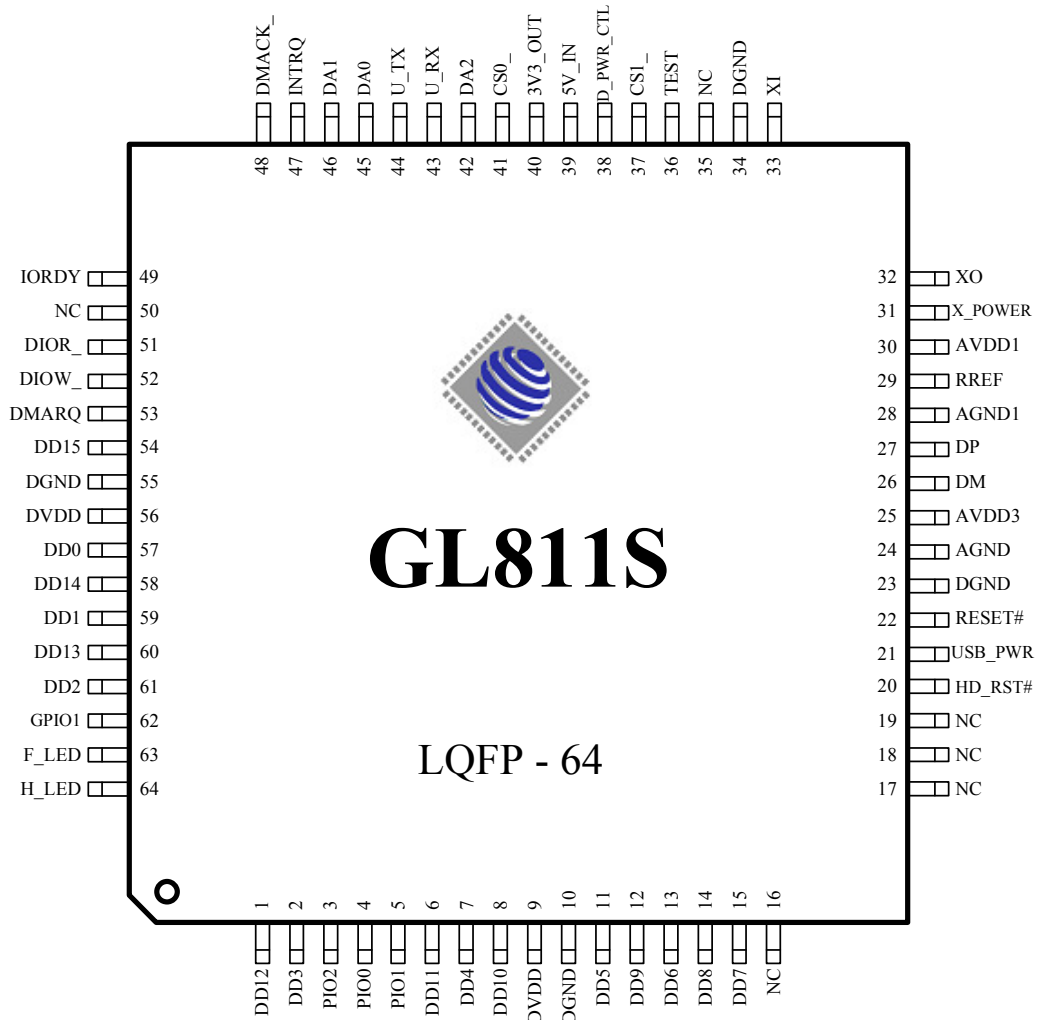


Figure 3.2 - 64 Pin LQFP Pinout Diagram



3.2 Pin List

Table 3.1 - 48 Pin List

| Pin# | Pin Name | Type | Pin# | Pin Name | Type | Pin# | Pin Name | Type | Pin# | Pin Name | Type |
|------|----------|------|------|----------|------|------|-----------|------|------|----------|------|
| 1 | DD12 | B | 13 | HD_RST# | O | 25 | XI | I | 37 | IORDY | I |
| 2 | DD3 | B | 14 | USB_PWR | B | 26 | TEST | I | 38 | DIOR_ | O |
| 3 | PIO0 | B | 15 | RESET# | I | 27 | CS1_ | O | 39 | DIOW_ | O |
| 4 | DD11 | B | 16 | AGND1 | P | 28 | D_PWR_CTL | B | 40 | DMARQ | I |
| 5 | DD4 | B | 17 | AVDD1 | P | 29 | 5V_IN | P | 41 | DD15 | B |
| 6 | DD10 | B | 18 | DM | B | 30 | 3V3_OUT | P | 42 | DVDD | P |
| 7 | DVDD1 | P | 19 | DP | B | 31 | CS0_ | O | 43 | DD0 | B |
| 8 | DD5 | B | 20 | AGND2 | P | 32 | DA2 | O | 44 | DD14 | B |
| 9 | DD9 | B | 21 | VREF | A | 33 | DA0 | O | 45 | DD1 | B |
| 10 | DD6 | B | 22 | AVCC2 | P | 34 | DA1 | O | 46 | DD13 | B |
| 11 | DD8 | B | 23 | X-POWER | P | 35 | INTRQ | I | 47 | DD2 | B |
| 12 | DD7 | B | 24 | XO | B | 36 | DMACK_ | O | 48 | GPIO1 | B |

Table 3.2 - 64 Pin List

| Pin# | Pin Name | Type | Pin# | Pin Name | Type | Pin# | Pin Name | Type | Pin# | Pin Name | Type |
|------|----------|------|------|----------|------|------|-----------|------|------|----------|------|
| 1 | DD12 | B | 17 | NC | | 33 | XI | I | 49 | IORDY | I |
| 2 | DD3 | B | 18 | NC | | 34 | DGND | P | 50 | NC | |
| 3 | PIO2 | B | 19 | NC | | 35 | NC | | 51 | DIOR_ | O |
| 4 | PIO0 | B | 20 | HD_RST# | O | 36 | TEST | I | 52 | DIOW_ | O |
| 5 | PIO1 | B | 21 | USB_PWR | B | 37 | CS1_ | O | 53 | DMARQ | I |
| 6 | DD11 | B | 22 | RESET# | I | 38 | D_PWR_CTL | B | 54 | DD15 | B |
| 7 | DD4 | B | 23 | DGND | P | 39 | 5V_IN | P | 55 | DGND | P |
| 8 | DD10 | B | 24 | AGND | P | 40 | DVDD | P | 56 | DVDD | P |
| 9 | DVDD | P | 25 | AVDD3 | P | 41 | CS0_ | O | 57 | DD0 | B |
| 10 | DGND | P | 26 | DM | B | 42 | DA2 | O | 58 | DD14 | B |
| 11 | DD5 | B | 27 | DP | B | 43 | U_RX | B | 59 | DD1 | B |
| 12 | DD9 | B | 28 | AGND1 | P | 44 | U_TX | O | 60 | DD13 | B |
| 13 | DD6 | B | 29 | RREF | A | 45 | DA0 | O | 61 | DD2 | B |
| 14 | DD8 | B | 30 | AVDD1 | P | 46 | DA1 | O | 62 | GPIO 1 | B |



| | | | | | | | | | | | |
|----|-----|---|----|---------|---|----|--------|---|----|-------|---|
| 15 | DD7 | B | 31 | X_POWER | P | 47 | INTRQ | I | 63 | F_LED | B |
| 16 | NC | | 32 | XO | B | 48 | DMACK_ | O | 64 | H_LED | B |

3.3 Pin Descriptions

Table 3.3 – 48 Pin Descriptions

| USB Interface | | | |
|---------------|------|--------|--------------------|
| Pin Name | Pin# | Type | Description |
| VREF | 21 | A | Reference Resistor |
| DM | 18 | B | HS D- |
| DP | 19 | B | HS D+ |
| XO | 24 | B | Crystal output |
| XI | 25 | I | Crystal input |
| RESET# | 15 | I (pu) | External reset |
| TEST | 26 | I (pd) | Test mode Input |

| ATA/ATAPI Interface | | | |
|---------------------|--|--------|----------------------|
| Pin Name | Pin# | Type | Description |
| DD0~15 | 43,45,47,2,5,8,10,12,11,9,6,4,1,46,44,41 | B (pd) | IDE Data Bus |
| HD_RST# | 13 | O | Device Reset |
| CS1_, CS0_ | 27,31 | O | Chip Select #1,#0 |
| DA0~2 | 33,34,32 | O | IDE Address #2,#1,#0 |
| INTRQ | 35 | I (pd) | IDE interrupt input |
| DMACK_ | 36 | O | IDE Acknowledge |
| IORDY | 37 | I (pu) | IDE Ready |
| DIOR_ | 38 | O | IDE read signal |
| DIOW_ | 39 | O | IDE write signal |
| DMARQ | 40 | I (pd) | IDE request |

| Miscellaneous Interface | | | |
|-------------------------|------|-----------|-------------|
| Pin Name | Pin# | Type | Description |
| GPIO 1 | 48 | B (pu) | GPIO |
| PIO0 | 3 | B (pd) | GPIO |

| Power / Ground | | | |
|-------------------------------------|------------|------|---------------|
| Pin Name | Pin# | Type | Description |
| 5V_IN | 29 | P | 5V input |
| DVDD1,X-POWER, 3V3_OUT, DVDD2 | 7,23,30,42 | P | Digital VDD |
| AGND1 | 16 | P | Analog GND |
| AGND2 | 20 | P | Analog GND #1 |
| AVCC1 | 17 | P | Analog VDD #3 |
| AVCC2 | 22 | P | Analog VDD #1 |

| Miscellaneous | | | |
|---------------|------|-----------|-------------------|
| Pin Name | Pin# | Type | Description |
| USB_PWR | 14 | B (pu) | USB power detect |
| D_PWR_CTL | 28 | B (pd) | HDD power control |

Table 3.4 - 64 Pin Descriptions

| USB Interface | | | |
|---------------|------|-----------|--------------------|
| Pin Name | Pin# | Type | Description |
| RREF | 29 | A | Reference Resistor |
| DM | 26 | B | HS D- |
| DP | 27 | B | HS D+ |
| XO | 32 | B | Crystal output |
| XI | 33 | I | Crystal input |
| RESET# | 22 | I (pu) | External reset |
| TEST | 36 | I (pd) | Test mode Input |

| ATA/ATAPI Interface | | | |
|---------------------|--|-----------|----------------------|
| Pin Name | Pin# | Type | Description |
| DD0~15 | 57,59,61, 2,7,11,13, 15,14,12, 8,6,1,60, 58,54 | B (pd) | IDE Data Bus |
| HD_RST# | 20 | O | Device Reset |
| CS1_, CS0_ | 37,41 | O | Chip Select #1,#0 |
| DA0~2 | 45,46,42 | O | IDE Address #2,#1,#0 |
| INTRQ | 47 | I (pd) | IDE interrupt input |
| DMACK_ | 48 | O | IDE Acknowledge |
| IORDY | 49 | I (pu) | IDE Ready |
| DIOR_ | 51 | O | IDE read signal |
| DIOW_ | 52 | O | IDE write signal |
| DMARQ | 53 | I (pd) | IDE request |

| Miscellaneous Interface | | | |
|-------------------------|------|-----------|---|
| Pin Name | Pin# | Type | Description |
| GOPI 1 | 62 | B (pu) | General Purpose IO #1 |
| PIO 0 | 4 | B (pd) | Program IO #0 |
| PIO 1 | 5 | B (pd) | Program IO #1 becomes SPIDI when SPI interface is enabled (SPIDI : SPI Data Input) |
| PIO 2 | 3 | B (pd) | Program I/O #2 becomes SPIDO when SPI interface is enabled (SPIDO : SPI Data Output) |
| U_RX | 43 | B (pu) | UART RXD |
| U_TX | 44 | O | UART TXD |

| Power / Ground | | | |
|----------------|-------------|------|---------------|
| Pin Name | Pin# | Type | Description |
| 5V_IN | 39 | P | 5V input |
| DGND | 10,23,34,55 | P | Digital GND |
| DVDD | 9,31,40,56 | P | Digital VDD |
| AGND | 24 | P | Analog GND |
| AGND1 | 28 | P | Analog GND #1 |
| AVDD3 | 25 | P | Analog VDD #3 |



| | | | |
|-------|----|---|---------------|
| AVDD1 | 30 | P | Analog VDD #1 |
|-------|----|---|---------------|

| Miscellaneous | | | |
|---------------|------|-----------|---------------------------------------|
| Pin Name | Pin# | Type | Description |
| USB_PWR | 21 | B (pu) | USB power detect |
| F_LED | 63 | B (pu) | Operation mode indicator (Full-Speed) |
| H_LED | 64 | B (pu) | Operation mode indicator (High-Speed) |
| D_PWR_CTL | 38 | B (pd) | HDD power control |

Notation:

| | | |
|-------------|-------------|-----------------------------------|
| Type | O | Output |
| | I | Input |
| | B | Bi-directional |
| | B/I | Bi-directional, default input |
| | B/O | Bi-directional, default output |
| | P | Power / Ground |
| | A | Analog |
| | SO | Automatic output low when suspend |
| | pu | Internal pull up |
| | pd | Internal pull down |
| | odpu | Open drain with internal pull up |

CHAPTER 4 BLOCK DIAGRAM

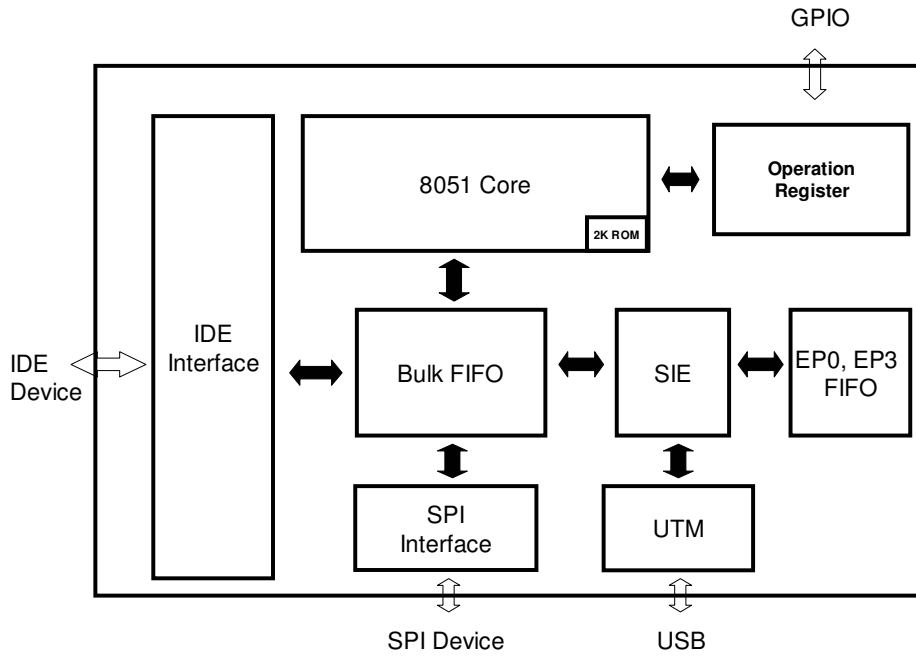


Figure 4.1 - Block Diagram



CHAPTER 5 FUNCTION DESCRIPTION

5.1 UTM

The USB 2.0 Transceiver Macrocell, it's the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic.

5.2 SIE

The Serial Interface Engine, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

5.3 EP0/EP3 FIFO

Endpoint 0/3 FIFO: The Control and Interrupt FIFO. It is composed of TX03FIFO and RX03FIFO, with 64-byte FIFO each, and it is used for endpoint 0/3 data transfer.

5.4 Bulk FIFO

It is constructed in interleaved architecture and composed by two data buffers which is used to store data transferred between USB host and IDE device.

5.5 IDE Interface

The IDE engine is extended from standard ATA / ATAPI protocol. It supports multiword DMA mode, and ultra DMA mode data transfers.

5.6 Operation Register

It is a register space to store status information and to control the functions of GL811S by 8051.

5.7 SPI Interface

The Serial Peripheral Interface is a serial, synchronous communication protocol. It is compatible with Motorola's SPI specifications.

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Table 6.1 - Maximum Ratings

| Symbol | Parameter | Min. | Max. | Unit |
|--------------------|-------------------------------------|------|-----------------------|------|
| V _{CC} | DC supply voltage | +3.0 | +3.6 | V |
| V _I | DC input voltage | -0.3 | V _{CC} + 0.3 | V |
| V _{I/O} | DC input voltage range for I/O | -0.3 | V _{CC} + 0.3 | V |
| V _{A/I/O} | DC input voltage for USB D+/D- pins | -0.3 | V _{CC} + 0.3 | V |
| V _{ESD} | Static discharge voltage | 4000 | | V |
| T _A | Ambient Temperature | 0 | 100 | °C |

6.2 Temperature Conditions

Table 6.2 - Temperature Conditions

| Item | Value |
|-----------------------|---------------|
| Storage Temperature | -50°C ~ 150°C |
| Operating Temperature | 0°C ~ 70°C |

6.3 DC Characteristics

6.3.1 I/O Type digital pins

Table 6.3 - I/O Type digital pins

| Parameter | Min. | Typ. | Max. | Unit |
|--|--------|--------|---------|------|
| Current sink @ V _{OL} = 0.4V | 10.58 | 14.21 | 16.87 | mA |
| Current output @ V _{OH} = 2.4V (TTL high) | 14.74 | 27.46 | 43.0 | mA |
| Falling slew rate at 30 pF loading capacitance | 0.56 | 0.91 | 1.28 | V/ns |
| Rising slew rate at 30 pF loading capacitance | 0.58 | 0.91 | 1.72 | V/ns |
| Schmitt trigger low to high threshold point | 1.4 | 1.5 | 1.6 | V |
| Schmitt trigger low to high threshold point | 1.4 | 1.5 | 1.6 | V |
| Pad internal pull up resister | 37.87K | 64.7K | 108.11K | Ohms |
| Pad internal pull down resister | 29.85K | 59.45K | 134.26K | Ohms |

6.3.2 D+/ D-

Table 6.4 - D+/ D-

| Parameter | Min. | Typ. | Max. | Unit |
|---|------|------|------|---------|
| D+/D- static output LOW (R_L of 1.5K to V_{CC}) | 0 | | 0.3 | V |
| D+/D- static output HIGH (R_L of 15K to GND) | 2.8 | | 3.6 | V |
| Differential input sensitivity | 0.2 | | | V |
| Single-ended receiver threshold | 0.8 | | 2.0 | V |
| Transceiver capacitance | | | 20 | pF |
| Hi-Z state data line leakage | -10 | | +10 | μ A |
| Driver output resistance | 28 | | 43 | Ohms |

6.3.3 Switching Characteristics

Table 6.5 - Switching Characteristics

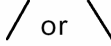
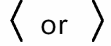


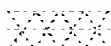

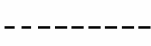
| Parameter | Min. | Typ. | Max. | Unit |
|-----------------------------------|-------|------|-------|------|
| X1 crystal frequency | 11.97 | 12 | 12.03 | MHz |
| X1 cycle time | | 83.3 | | ns |
| D+/D- rise time with 50pF loading | 4 | | 20 | ns |
| D+/D- fall time with 50pF loading | 4 | | 20 | ns |

6.4 AC Characteristics- ATA/ ATAPI

The GL811S complies with ATA / ATAPI-6 specification rev 1.0, which supports following data transfer modes:

1. DMA (Direct Memory Access) data transfer:
 DMA data transfer means of data transfer between device and host memory without host processor intervention.
 - Multiword DMA: Multiword DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When a Multiword DMA transfer is enabled as indicated by IDENTIFY DEVICE or IDENTIFY PACKET DEVICE data, this data transfer protocol shall be used for the data transfers associated with these commands. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)
 - Ultra DMA: Ultra DMA Is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA QUEUED, WRITE DMA QUEUED and PACKET commands. When this protocol is enabled, the Ultra DMA protocol shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. (Please refer to the ATA / ATAPI-6 specification rev 1.0 for more information.)

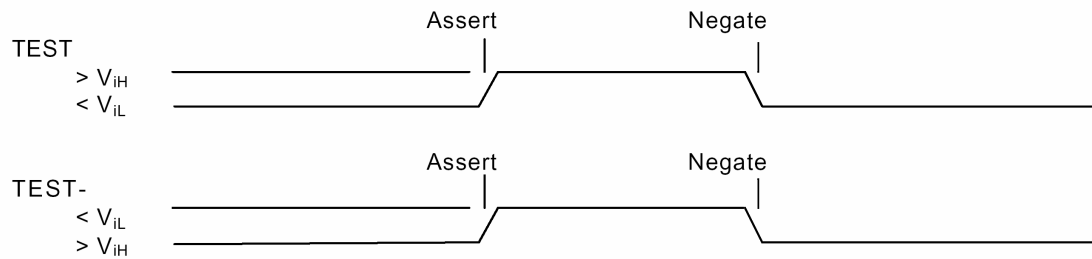
Following listed the symbols and their respective definitions that are used in the timing diagram:

| | |
|---|---|
|  | - Signal transition (asserted or negated) |
|  | - Data transition (asserted or negated) |
|  | - Data valid |
|  | - Undefined but not necessarily released |
|  | - Asserted, negated or released |
|  | - Released |
|  | - The "other" condition if a signal is shown with no change |

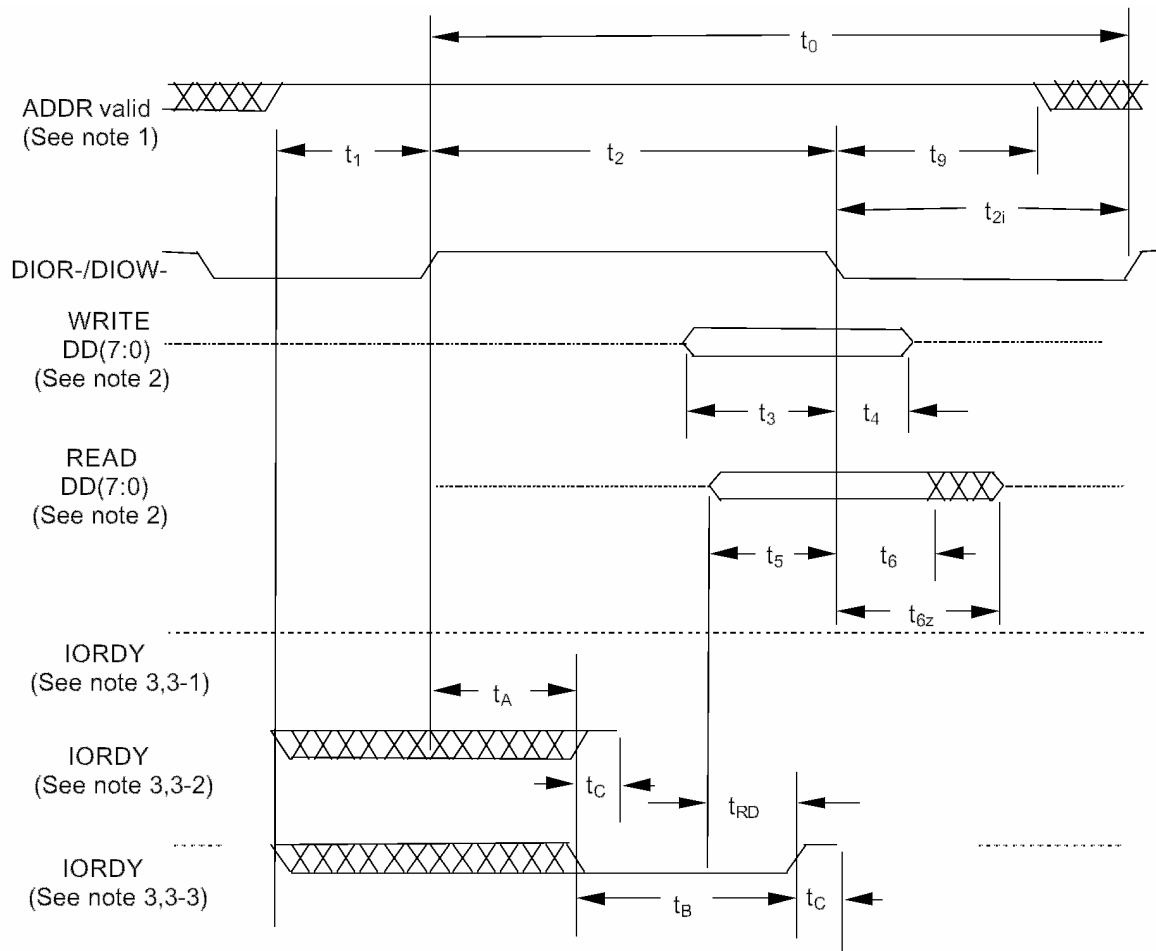
All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted. The following illustrates the representation of a signal named Test going from negated to asserted and back to negated, based on the polarity of the signal.



6.4.1 Register Transfers / PIO Data Transfers



Notes:

1. Device address consists of signals CS0_, CS1_ and DA(2:0).
2. Data consists of IODD(7:0).
3. The negation of IORDY by the device is used to extend the register transfer cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR_ or DIOW_. The assertion and negation of IORDY are described as following:
 - 3.1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
 - 3.2 Device negates IORDY before t_A , but causes IORDY to be asserted before t_A . IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
 - 3.3 Device negates IORDY before t_A , IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is released. For cycles where a wait is generated and DIOR_ is asserted, the device shall read data on IODD(0:7) for t_{RD} before asserting IORDY.
4. DMACK_ shall remain negated during a register transfer.



GL811S USB2.0 to ATA/ATAPI Bridge Controller

| Register transfer timing parameters | | Mode 0 ns | Mode 1 ns | Mode 2 ns | Mode 3 ns | Mode 4 ns | Note |
|-------------------------------------|---|--------------|--------------|--------------|--------------|--------------|-------|
| t_0 | Cycle time (min) | 600 | 383 | 330 | 180 | 120 | 1,4,5 |
| t_1 | Address valid to DIOR-/DIOw- setup (min) | 70 | 50 | 30 | 30 | 25 | |
| t_2 | DIOR-/DIOw- pulse width 8-bit (min) | 290 | 290 | 290 | 80 | 70 | 1 |
| $t_{2\bar{z}}$ | DIOR-/DIOw- recovery time (min) | - | - | - | 70 | 25 | 1 |
| t_3 | DIOw- data setup (min) | 60 | 45 | 30 | 30 | 20 | |
| t_4 | DIOw- data hold (min) | 30 | 20 | 15 | 10 | 10 | |
| t_5 | DIOR- data setup (min) | 50 | 35 | 20 | 20 | 20 | |
| t_6 | DIOR- data hold (min) | 5 | 5 | 5 | 5 | 5 | |
| $t_{6\bar{z}}$ | DIOR- data release (max) | 30 | 30 | 30 | 30 | 30 | 2 |
| t_9 | DIOR-/DIOw- to address valid hold (min) | 20 | 15 | 10 | 10 | 10 | |
| t_{RD} | Read Data Valid to IORDY active (if IORDY initially low after t_A) (min) | 0 | 0 | 0 | 0 | 0 | |
| t_A | IORDY Setup time | 35 | 35 | 35 | 35 | 35 | 3 |
| t_B | IORDY Pulse Width (max) | 1250 | 1250 | 1250 | 1250 | 1250 | |
| t_C | IORDY assertion to release (max) | 5 | 5 | 5 | 5 | 5 | |

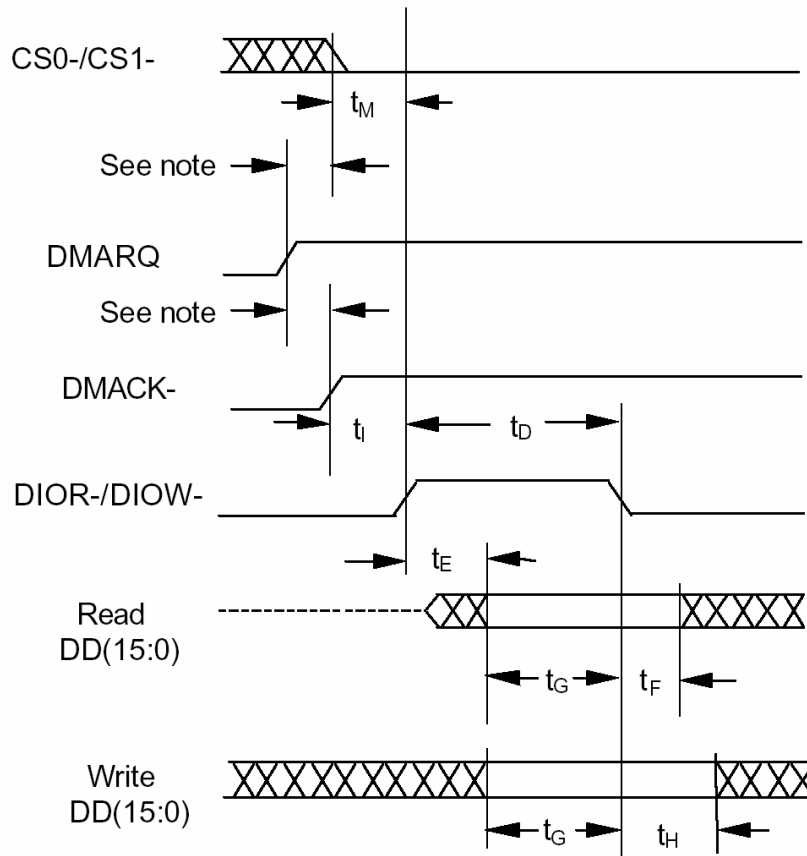
NOTES -

- 1 t_0 is the minimum total cycle time, t_2 is the minimum DIOR-/DIOw- assertion time, and $t_{\bar{z}}$ is the minimum DIOR-/DIOw- negation time. A host implementation shall lengthen $t_{\bar{z}}$ and/or t_2 to ensure that t_0 is equal to or greater than the value reported in the devices IDENTIFY DEVICE data. A device implementation shall support any legal host implementation.
- 2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is released by the device.
- 3 The delay from the activation of DIOR- or DIOw- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the register transfer cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOw-, then t_5 shall be met and t_{RD} is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOw-, then t_{RD} shall be met and t_5 is not applicable.
- 4 ATA/ATAPI standards prior to ATA/ATAPI-5 inadvertently specified an incorrect value for mode 2 time t_5 by utilizing the 16-bit PIO value
- 5 Mode shall be selected no higher than the highest mode supported by the slowest device.

6.4.2 Multiword DMA data transfer

| Multiword DMA timing parameters | | Mode 0 ns | Mode 1 ns | Mode 2 ns | Note |
|---------------------------------|--|--------------|--------------|--------------|----------|
| t_0 | Cycle time (min) | 480 | 150 | 120 | see note |
| t_D | DIOR-/DIOW- asserted pulse width (min) | 215 | 80 | 70 | see note |
| t_E | DIOR- data access (max) | 150 | 60 | 50 | |
| t_F | DIOR- data hold (min) | 5 | 5 | 5 | |
| t_G | DIOR-/DIOW- data setup (min) | 100 | 30 | 20 | |
| t_H | DIOW- data hold (min) | 20 | 15 | 10 | |
| t_I | DMACK to DIOR-/DIOW- setup (min) | 0 | 0 | 0 | |
| t_J | DIOR-/DIOW- to DMACK hold (min) | 20 | 5 | 5 | |
| t_{KR} | DIOR- negated pulse width (min) | 50 | 50 | 25 | see note |
| t_{KW} | DIOW- negated pulse width (min) | 215 | 50 | 25 | see note |
| t_{LR} | DIOR- to DMARQ delay (max) | 120 | 40 | 35 | |
| t_{LW} | DIOW- to DMARQ delay (max) | 40 | 40 | 35 | |
| t_M | CS(1:0) valid to DIOR-/DIOW- (min) | 50 | 30 | 25 | |
| t_N | CS(1:0) hold (min) | 15 | 10 | 10 | |
| t_Z | DMACK- to read data released (max) | 20 | 25 | 25 | |

NOTE – t_0 is the minimum total cycle time, t_D is the minimum DIOR-/DIOW- assertion time, and t_k (t_{KR} or t_{KW} , as appropriate) is the minimum DIOR-/DIOW- negation time. A host shall lengthen t_D and/or t_k to ensure that t_0 is equal to the value reported in the devices IDENTIFY DEVICE data.



Note:

The host shall not assert DMACK_ or negate both CS0_ and CS1_ until the assertion of DMARQ is detected. The maximum time from the assertion of DMARQ to the assertion of DMACK_ or the negation of both CS0_ and CS1_ is not defined.

Figure 6.1 - Initiating a Multiword DMA Data Burst

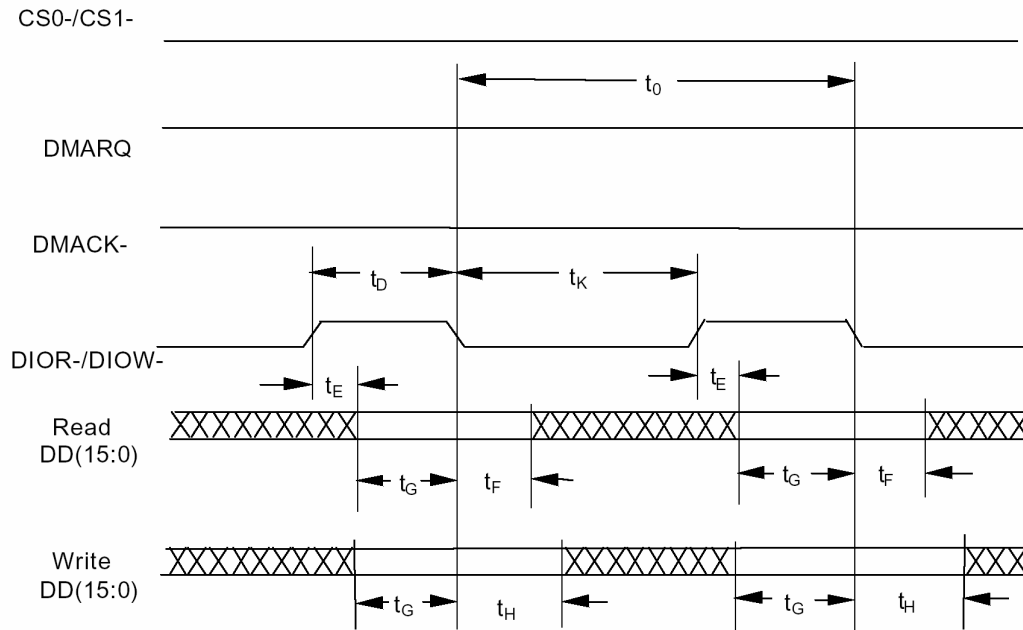
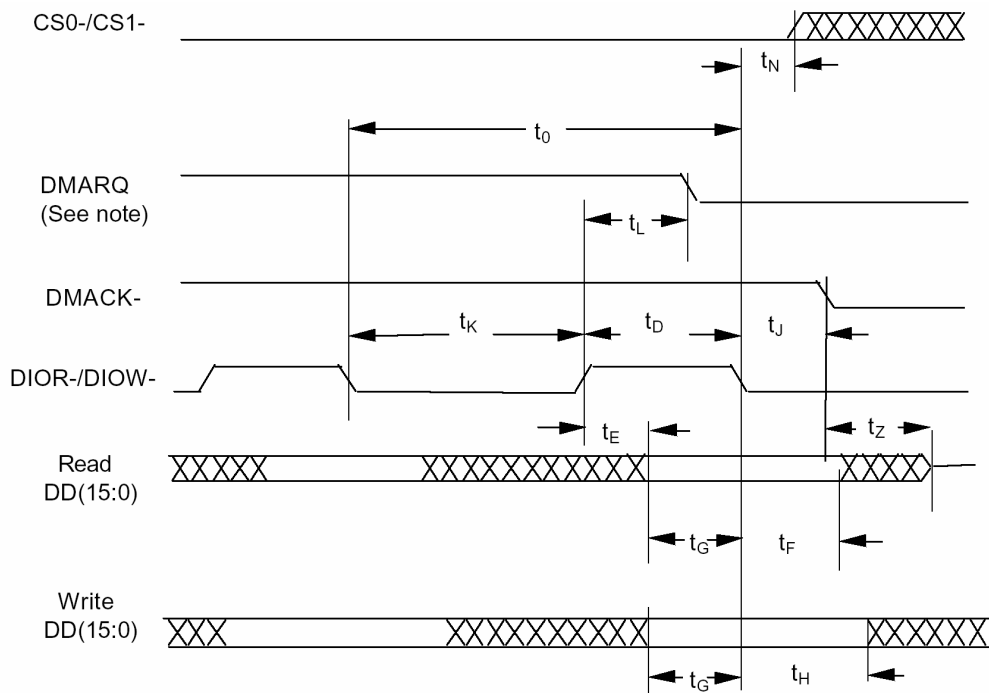


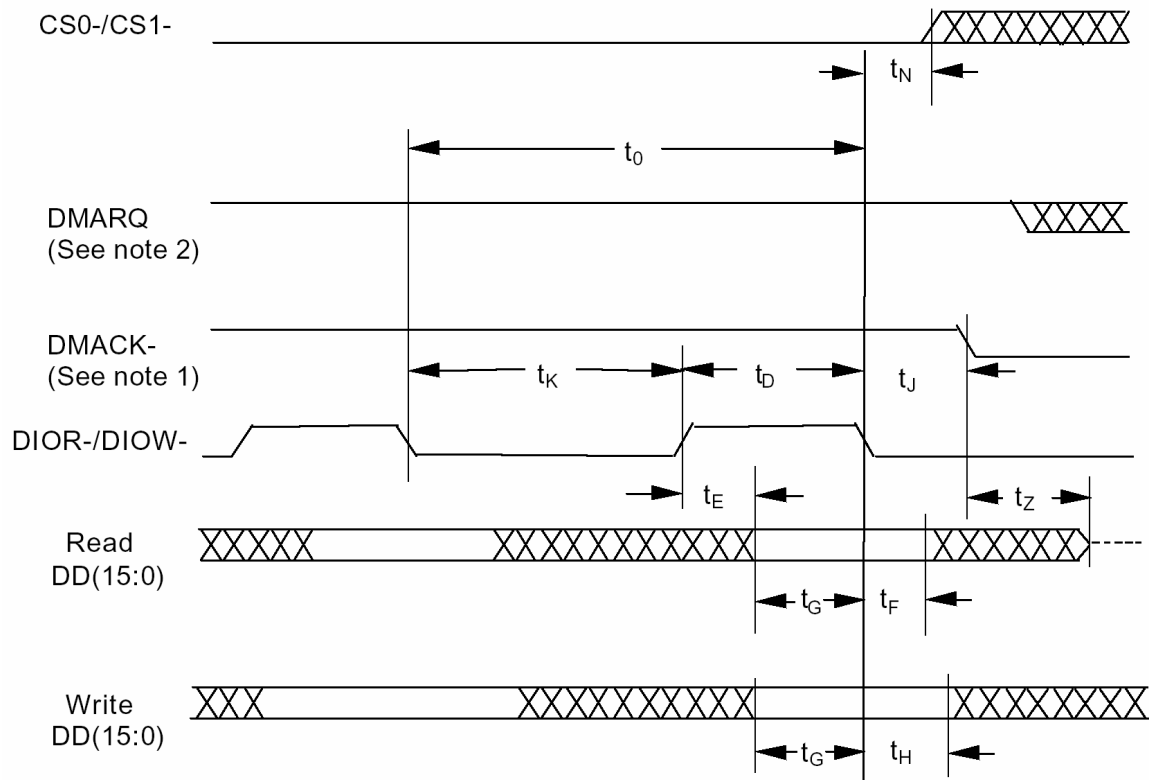
Figure 6.2 - Sustaining a Multiword DMA Data Burst



Note:

To terminate the data burst, the Device shall negate DMARQ within the t_L of the assertion of the current DIOR_ or DIOW_ pulse. The last data word for the burst shall then be transferred by the negation of the current DIOR_ or DIOW_ pulse. If all data for the command has not been transferred, the device shall reassert DMARQ again at any later time to resume the DMA operation.

Figure 6.3 - Device Terminating a Multiword DMA Data Burst



Note:

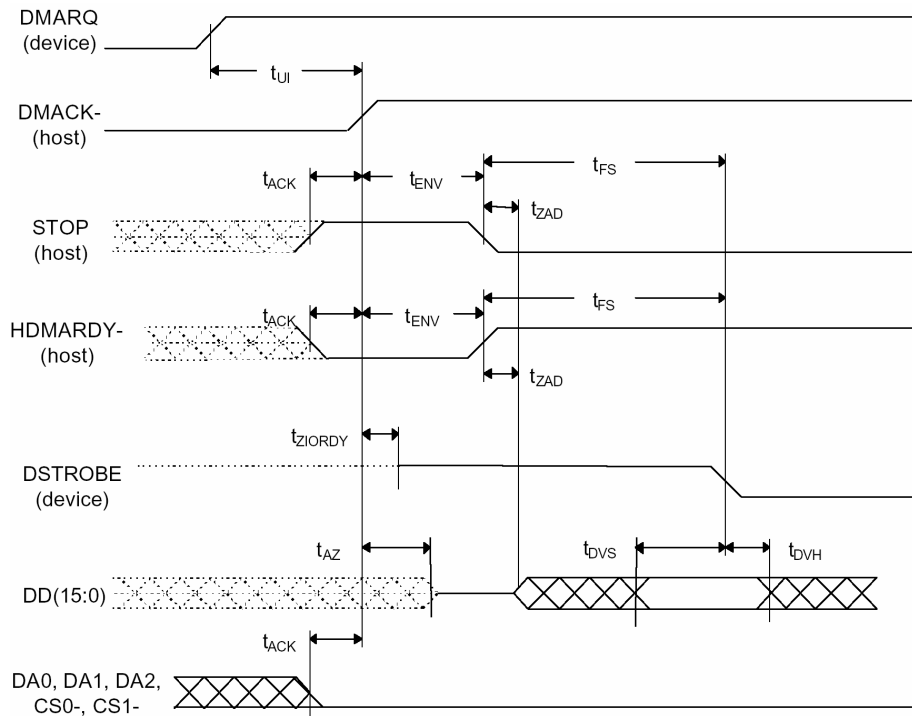
1. To terminate the transmission of a data burst, the Host shall negate DMACK_ within the specified time after a DIOR_ or DIOW_ pulse. No further DIOR_ or DIOW_ pulses shall be asserted for this burst.
2. If the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK_ or may negate DMARQ at any time after detecting that DMACK_ has been negated.

Figure 6.4 - Host terminating a Multiword DMA Data Burst

6.4.3 Ultra DMA data transfer

Table 6.5 - Ultra DMA data burst timing requirements

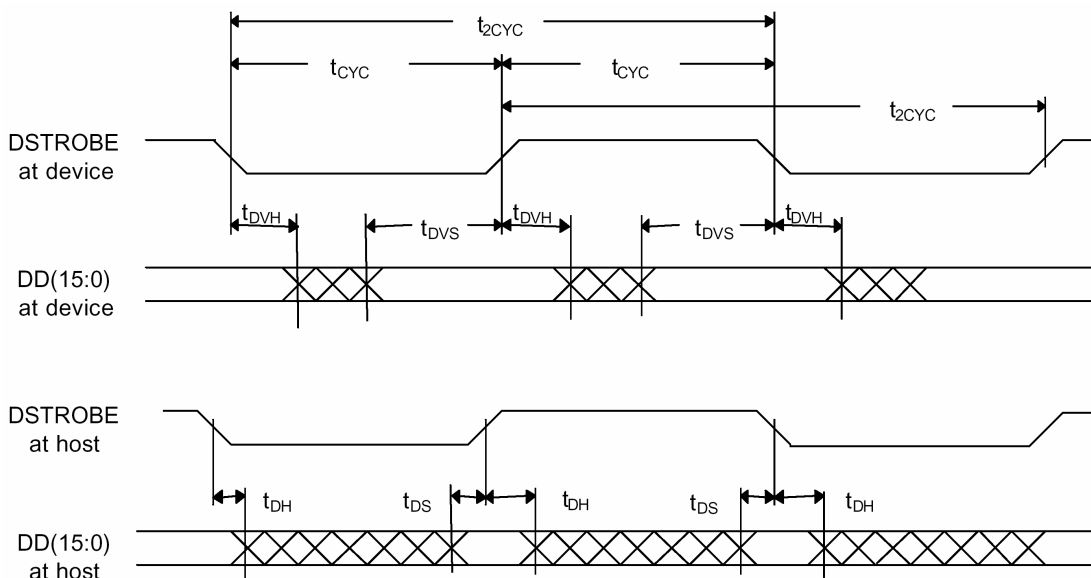
| Name | Mode 0 (in ns) | | Mode 1 (in ns) | | Mode 2 (in ns) | | Mode 3 (in ns) | | Mode 4 (in ns) | | Comment |
|---------------|-------------------|-----|-------------------|-----|-------------------|-----|-------------------|-----|-------------------|-----|---|
| | min | max | min | max | min | max | min | max | Min | max | |
| $t_{2CYCTYP}$ | 240 | | 160 | | 120 | | 90 | | 60 | | Typical sustained average two cycle time |
| t_{CYC} | 112 | | 73 | | 54 | | 39 | | 25 | | Cycle time allowing for asymmetry and clock variations |
| t_{2CYC} | 230 | | 154 | | 115 | | 86 | | 57 | | Two cycle time allowing for clock variations |
| t_{DS} | 15 | | 10 | | 7 | | 7 | | 5 | | Data setup time at recipient |
| t_{DH} | 5 | | 5 | | 5 | | 5 | | 5 | | Data hold time at recipient |
| t_{DVS} | 70 | | 48 | | 30 | | 20 | | 6 | | Data valid setup time at sender |
| t_{DVH} | 6 | | 6 | | 6 | | 6 | | 6 | | Data valid hold time at sender |
| t_{FS} | 0 | 230 | 0 | 200 | 0 | 170 | 0 | 130 | 0 | 120 | First STORBE time |
| t_{LI} | 0 | 150 | 0 | 150 | 0 | 150 | 0 | 100 | 0 | 100 | Limited interlock time |
| t_{MLI} | 20 | | 20 | | 20 | | 20 | | 20 | | Interlock time with minimum |
| t_{UI} | 0 | | 0 | | 0 | | 0 | | 0 | | Unlimited interlock time |
| t_{AZ} | | 10 | | 10 | | 10 | | 10 | | 10 | Maximum time allowed for output drivers to release |
| t_{ZAH} | 20 | | 20 | | 20 | | 20 | | 20 | | Minimum delay time required for output |
| t_{ZAD} | 0 | | 0 | | 0 | | 0 | | 0 | | Drivers to assert or negate |
| t_{ENV} | 20 | 70 | 20 | 70 | 20 | 70 | 20 | 55 | 20 | 55 | Envelope time |
| t_{SR} | | 50 | | 30 | | 20 | | NA | | NA | STROBE to DMARDY_ time |
| t_{RFS} | | 75 | | 70 | | 60 | | 60 | | 60 | Ready to final STROBE time |
| t_{RP} | 160 | | 125 | | 100 | | 100 | | 100 | | Minimum time to assert STOP or negate DMARQ |
| t_{IORDYZ} | | 20 | | 20 | | 20 | | 20 | | 20 | Maximum time before releasing IORDY |
| t_{ZIORDY} | 0 | | 0 | | 0 | | 0 | | 0 | | Minimum time before driving STROBE |
| t_{ACK} | 20 | | 20 | | 20 | | 20 | | 20 | | Setup and hold times for DMACK_ |
| t_{SS} | 50 | | 50 | | 50 | | 50 | | 50 | | Time from STROBE edge to negation of DMARQ or assertion of STOP |



Notes:

The definitions for the $DIOW_STOP$, $DIOR_HDMARDY_HSTROBE$ and $IORDY_DDMARDY_DSTROBE$ signal lines are not in efficient until $DMARQ$ and $DMACK$ are asserted.

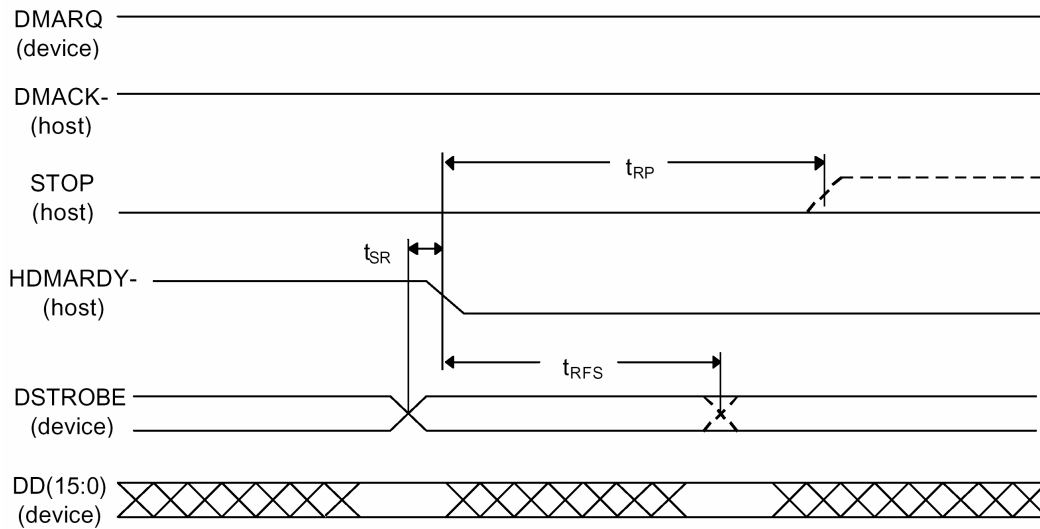
Figure 6.5 - Initiating an Ultra DMA Data-In Burst



Notes:

$IODD(15:0)$ and $DSTROBE$ signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

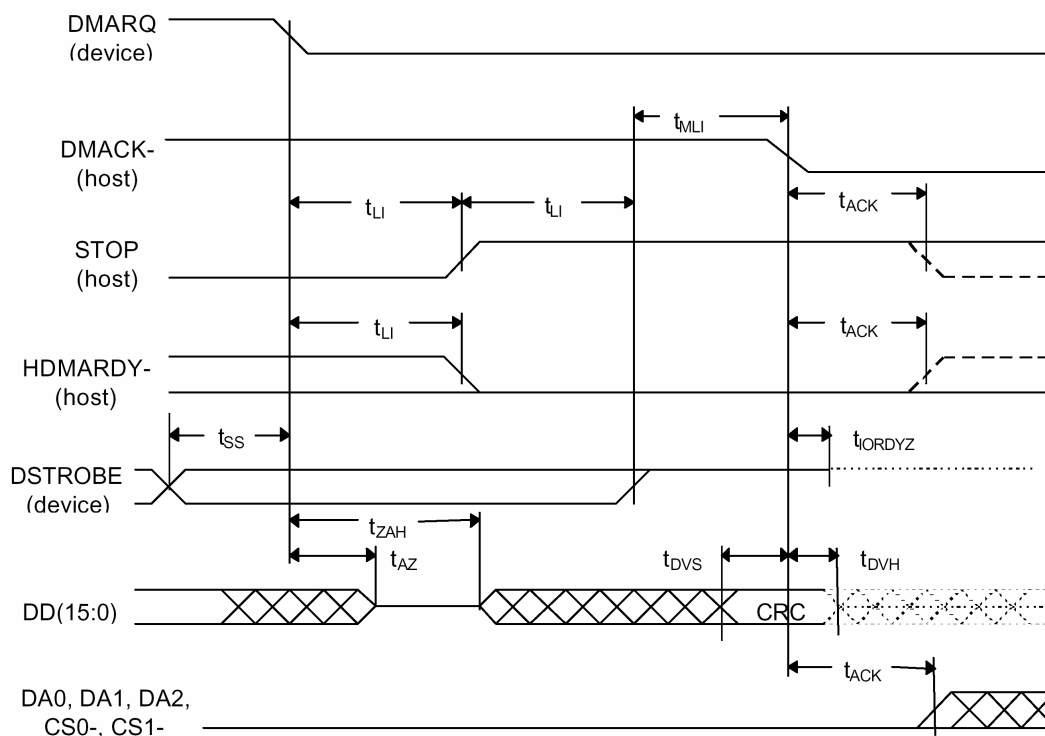
Figure 6.6 - Sustained Ultra DMA Data-In Burst



Notes:

1. The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the host may receive zero, one, or two more data words from the device.

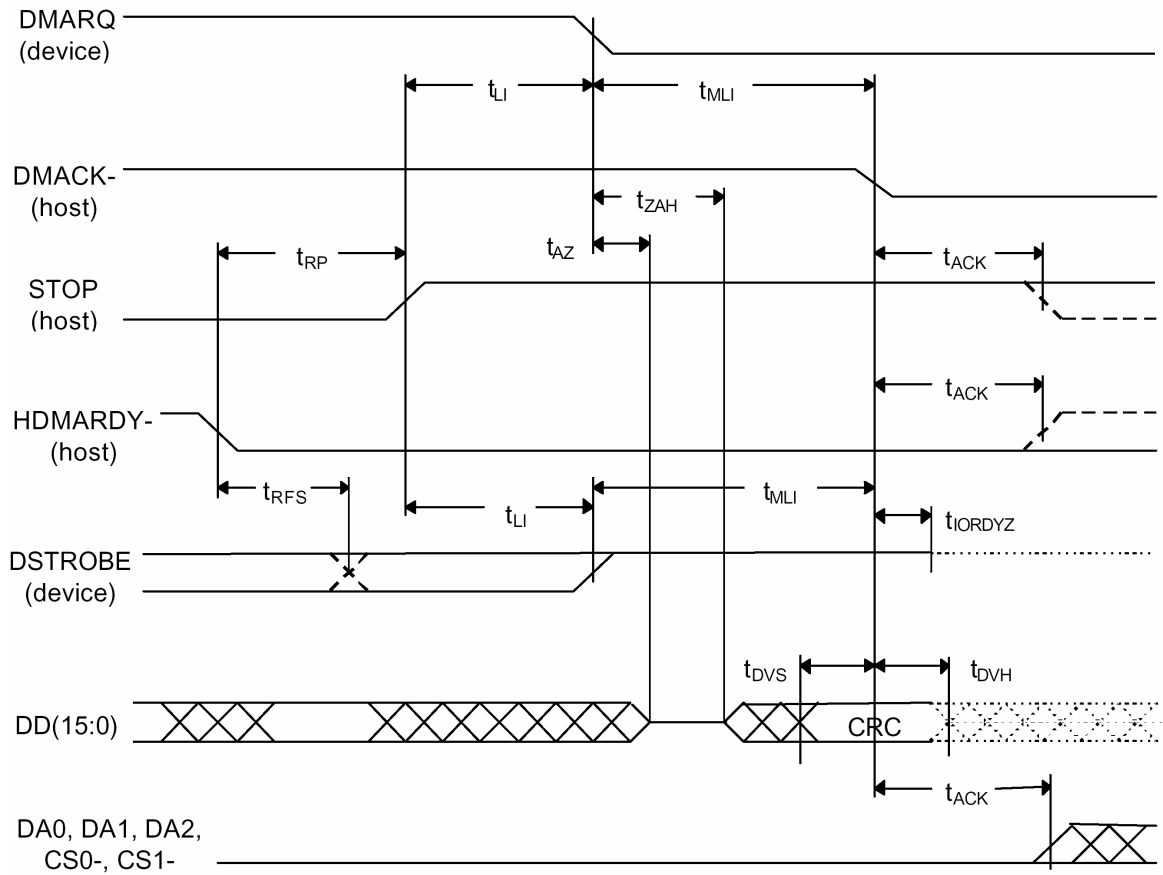
Figure 6.7 - Host Pausing an Ultra DMA Data-In Burst



Notes:

The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

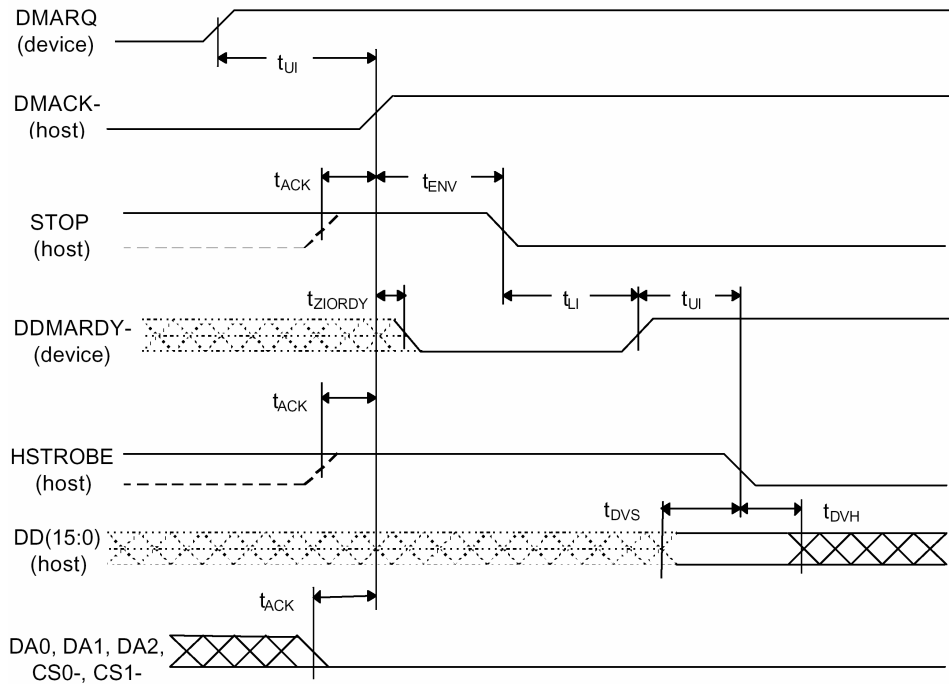
Figure 6.8 - Device Terminating an Ultra DMA Data-In Burst



Notes:

The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

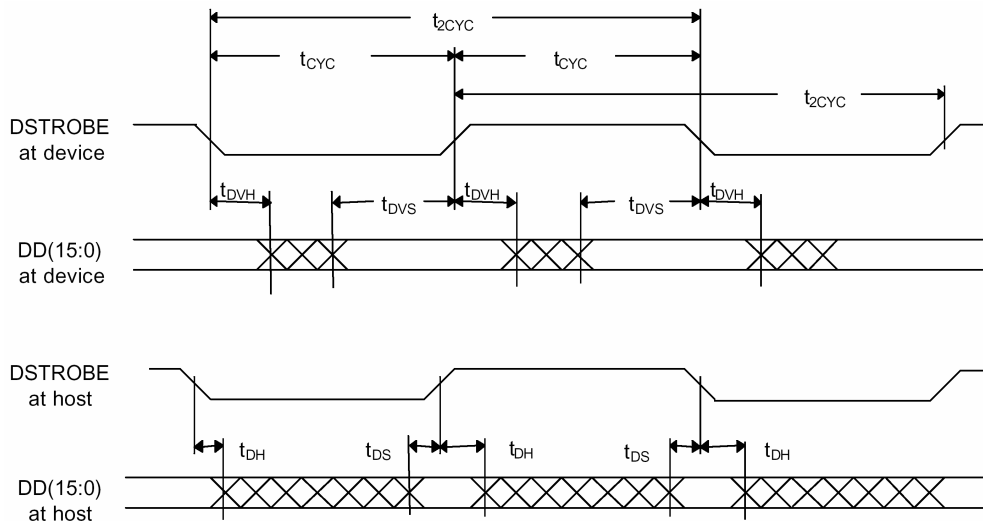
Figure 6.9 - Host Terminating an Ultra DMA Data-In Burst



Notes:

The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY_:DDMARDY_:DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

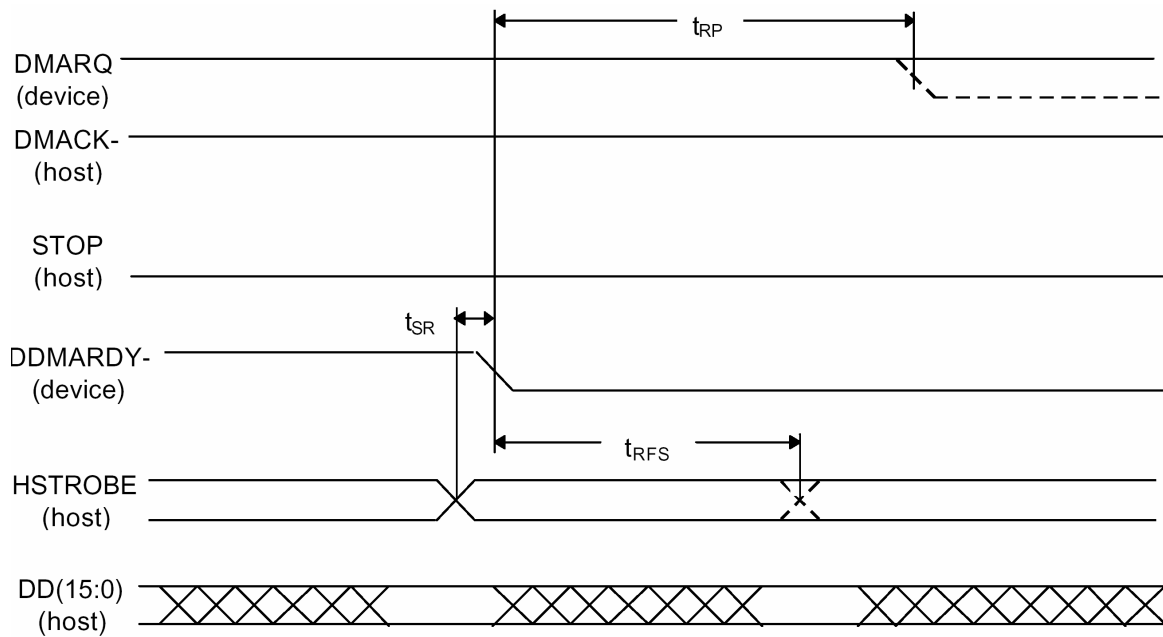
Figure 6.10 - Initiating an Ultra DMA Data-Out Burst



Notes:

IODD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

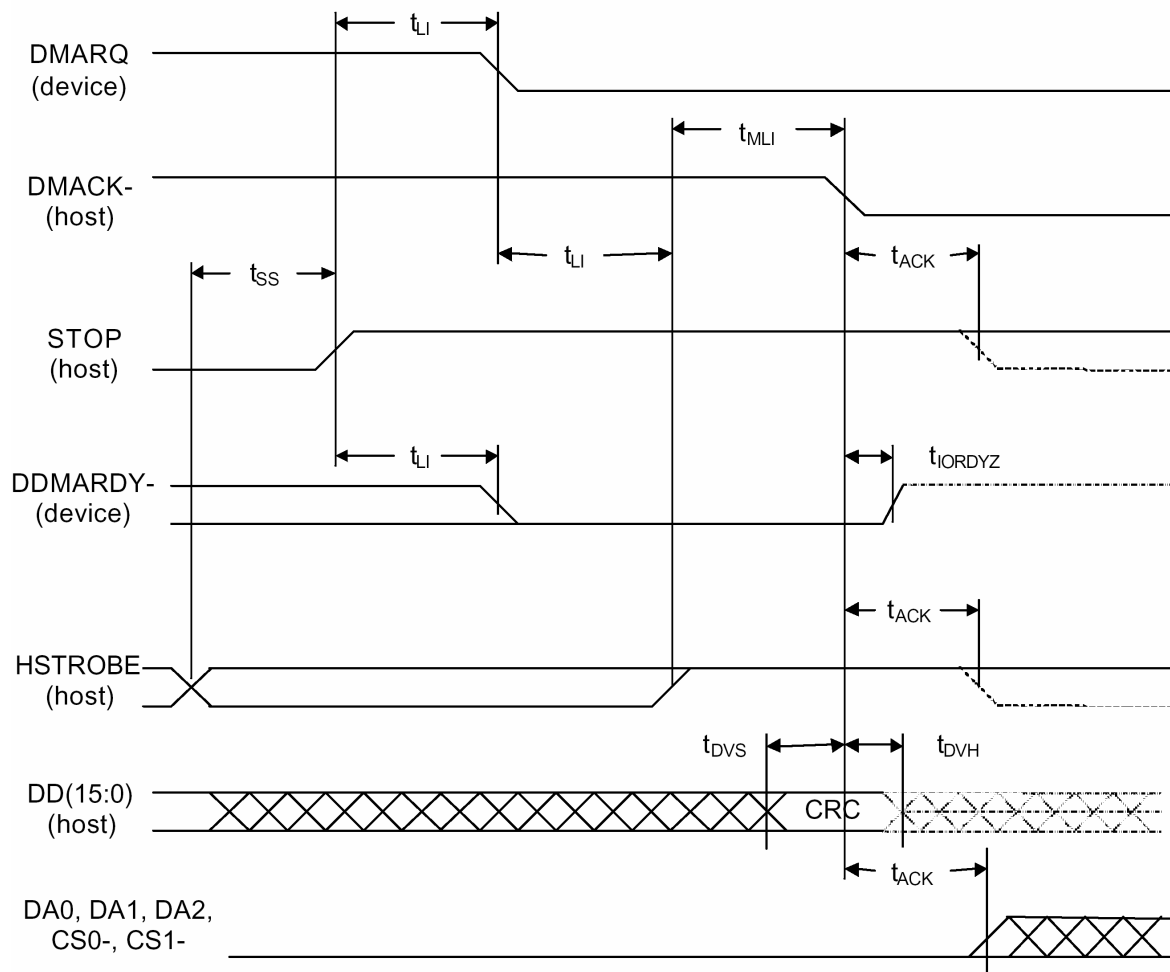
Figure 6.11 - Sustained Ultra DMA Data-Out Burst



Notes:

1. The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY_ is negated.
2. If the t_{SR} timing is not satisfied, the device may receive zero, one, or two more data words from the host.

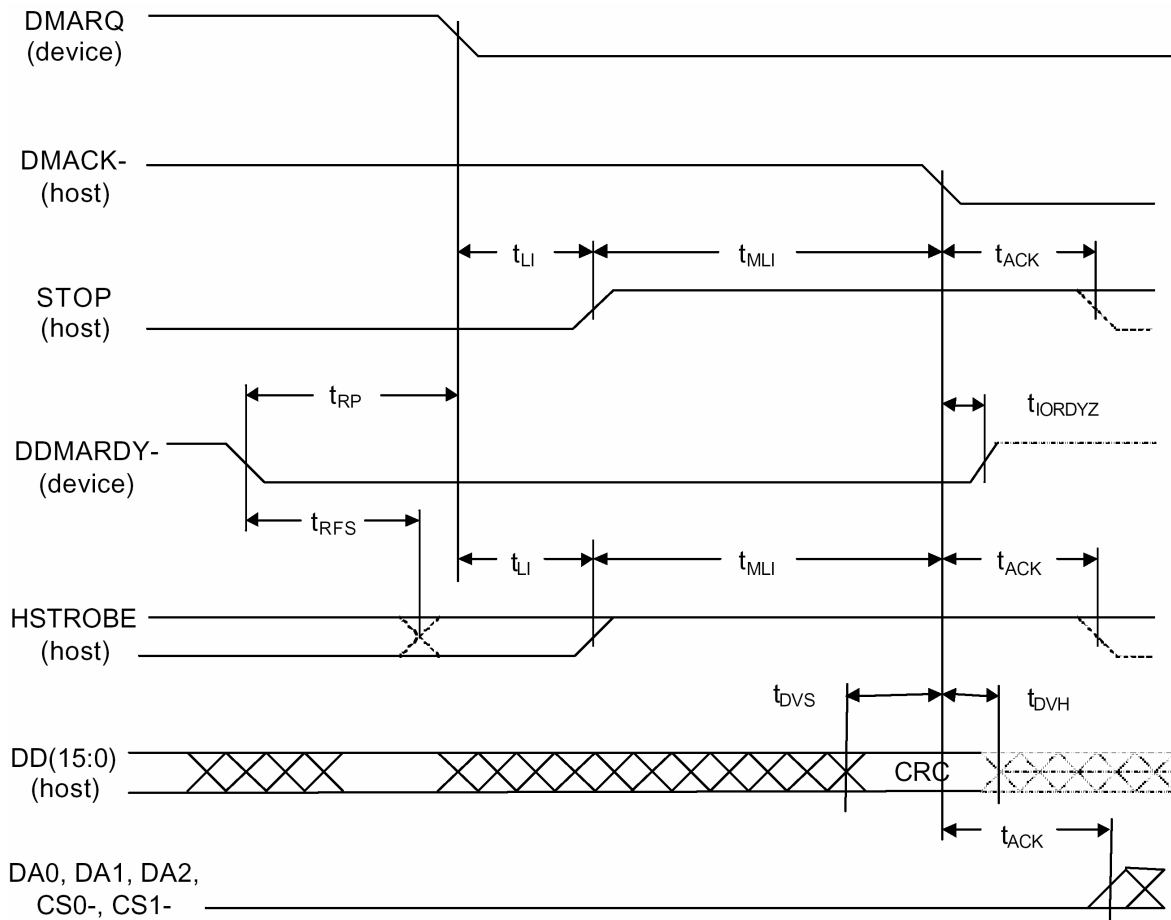
Figure 6.12 - Device Pausing an Ultra DMA Data-Out Burst



Notes:

The definitions for the DIOW_:STOP, DIOR_:HDMARDY_:HSTROBE and IORDY:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.13 - Host terminating an Ultra DMA data-out burst



Notes:

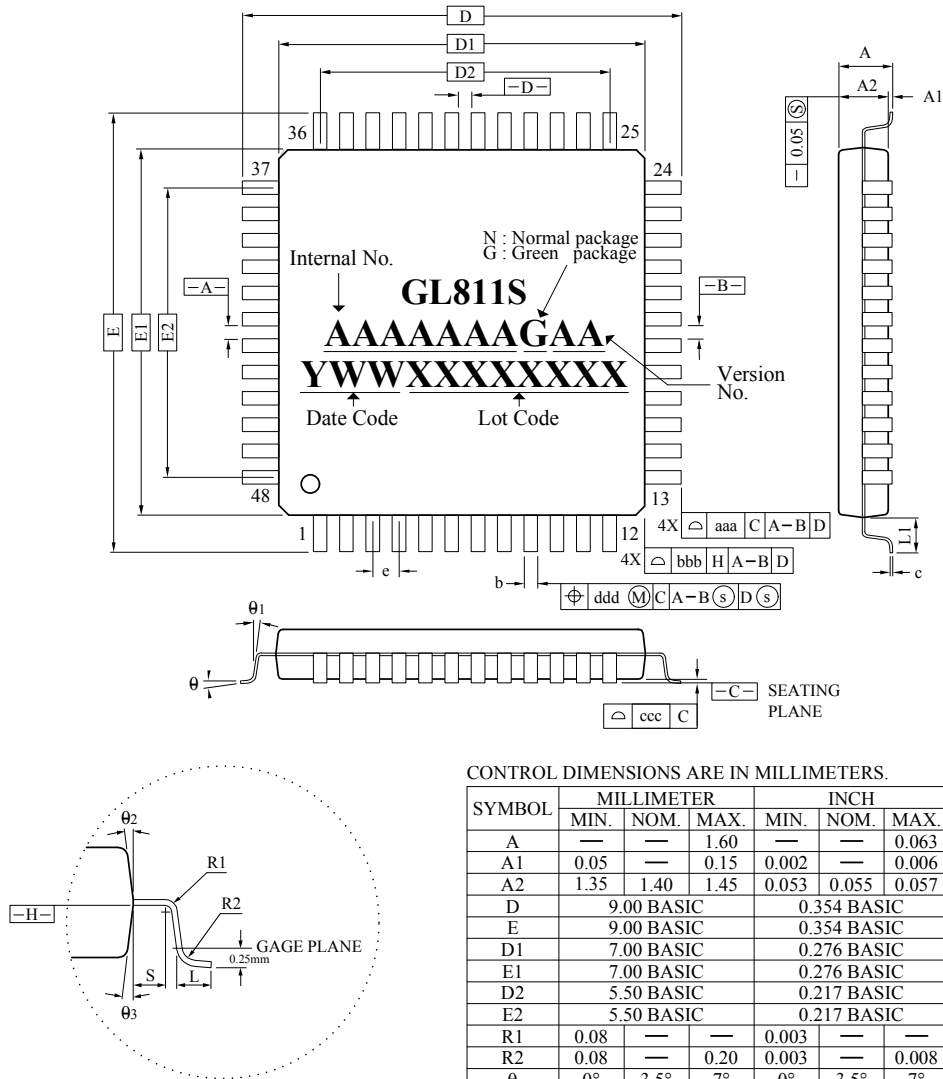
The definitions for the DIOW_:STOP, DIOR_:DDMARDY_:HSTROBE and IORDY_:DDMARDY_:DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 6.14 - Device Terminating an Ultra DMA Data-Out Burst

6.5 AC Characteristics - USB 2.0

The GL811S conforms to all timing diagrams and specifications for Universal Serial Bus specification rev. 2.0. Please refer to this specification for more information.

CHAPTER 7 PACKAGE DIMENSION



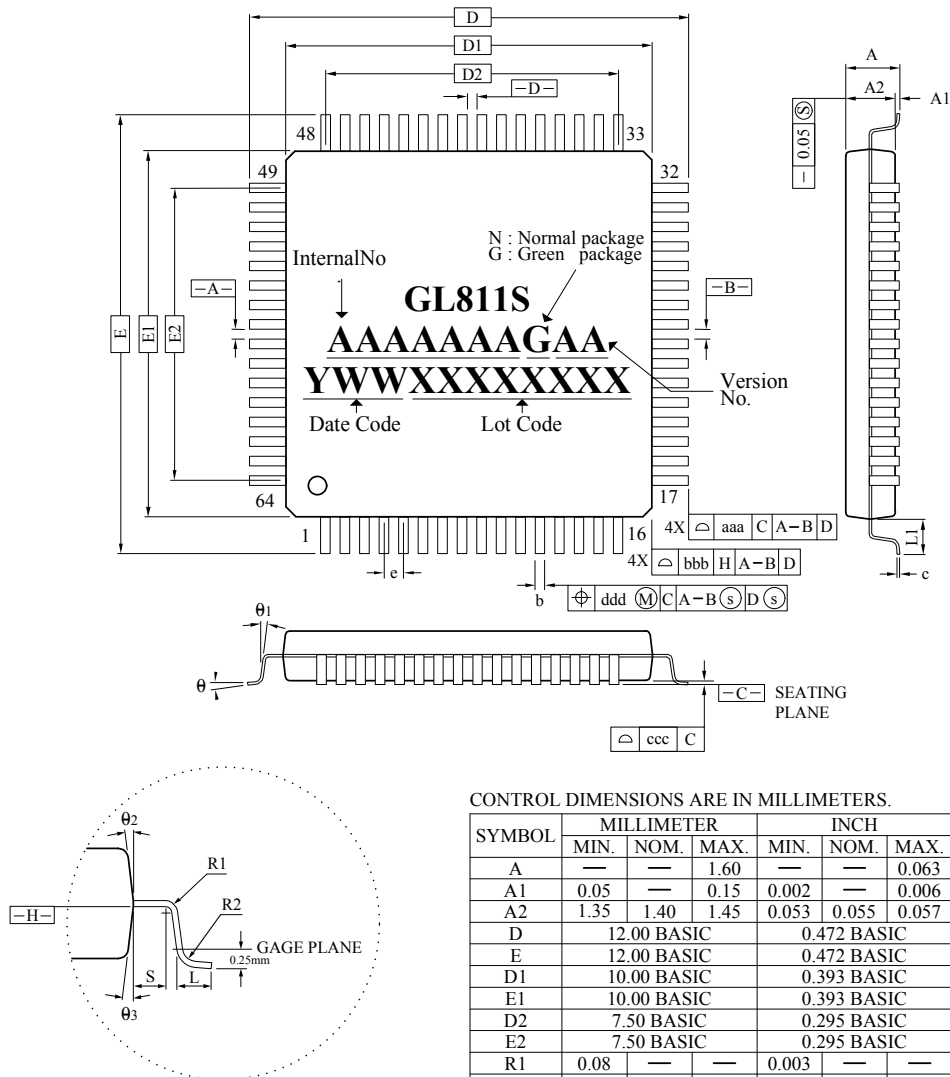
CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---------------------------------|------------|------|------|-------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 9.00 BASIC | | | 0.354 BASIC | | |
| E | 9.00 BASIC | | | 0.354 BASIC | | |
| D1 | 7.00 BASIC | | | 0.276 BASIC | | |
| E1 | 7.00 BASIC | | | 0.276 BASIC | | |
| D2 | 5.50 BASIC | | | 0.217 BASIC | | |
| E2 | 5.50 BASIC | | | 0.217 BASIC | | |
| R1 | 0.08 | — | — | 0.003 | — | — |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BASIC | | | 0.020 BASIC | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.1 – GL811S 48 Pin LQFP Package



CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---------------------------------|-------------|------|------|-------------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BASIC | | | 0.472 BASIC | | |
| E | 12.00 BASIC | | | 0.472 BASIC | | |
| D1 | 10.00 BASIC | | | 0.393 BASIC | | |
| E1 | 10.00 BASIC | | | 0.393 BASIC | | |
| D2 | 7.50 BASIC | | | 0.295 BASIC | | |
| E2 | 7.50 BASIC | | | 0.295 BASIC | | |
| R1 | 0.08 | — | — | 0.003 | — | — |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| θ | 0 | 3.5 | 7 | 0 | 3.5 | 7 |
| θ ₁ | 0 | — | — | 0 | — | — |
| θ ₂ | 11 | 12 | 13 | 11 | 12 | 13 |
| θ ₃ | 11 | 12 | 13 | 11 | 12 | 13 |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BASIC | | | 0.020 BASIC | | |
| TOLERANCES OF FORM AND POSITION | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

NOTES :

- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 7.2 – GL811S 64 Pin LQFP Package



CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

| Part Number | Package | Green | Version | Status |
|--------------|-------------|---------------|---------|-----------|
| GL811S-MNGXX | 48-pin LQFP | Green Package | XX | Available |
| GL811S-MSGXX | 64-pin LQFP | Green Package | XX | Available |