



**FEATURES**

- Fast access time : 8/10/12/15ns (max.)
- Low operating power consumption: 80 mA (typical.)
- Single 5V power supply
- All inputs and outputs are TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil skinny PDIP  
28-pin 300 mil SOJ  
28-pin 330 mil SOP  
28-pin 8mm×13.4 mm STSOP

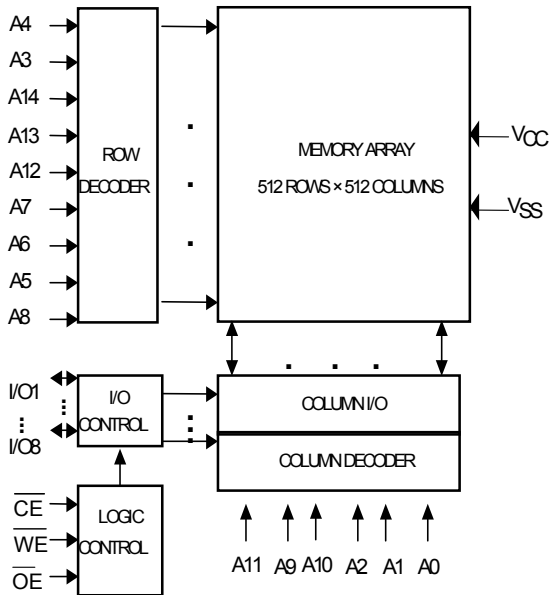
**GENERAL DESCRIPTION**

The UT61256 is a 262,144-bit high speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

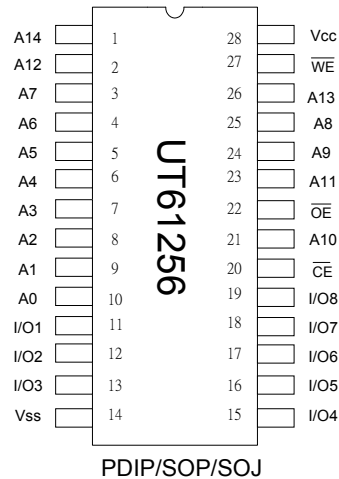
The UT61256 is designed for high-speed system application. It is particularly suited for use in high speed and high density system applications.

The UT61256 operates from a signal 5V power supply and all inputs and outputs are fully TTL compatible

**FUNCTIONAL BLOCK DIAGRAM**

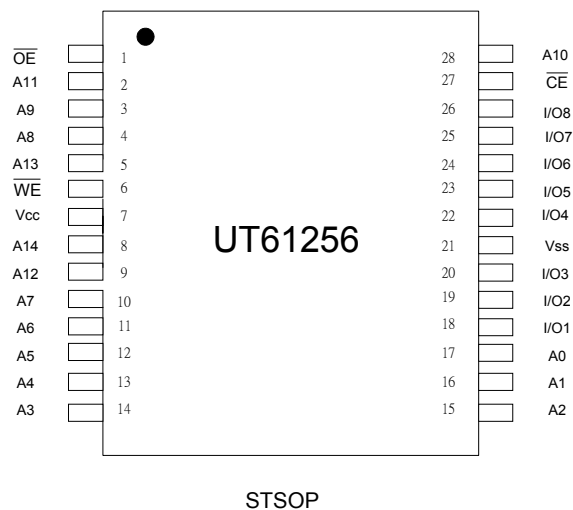


**PIN CONFIGURATION**



**PIN DESCRIPTION**

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V <sub>CC</sub>	Power Supply
V <sub>SS</sub>	Ground



**ABSOLUTE MAXIMUM RATINGS\***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to $V_{SS}$	$V_{TERM}$	-0.5 to +7.0	V
Operating Temperature	$T_A$	0 to +70	°C
Storage Temperature	$T_{STG}$	-65 to +150	°C
Power Dissipation	$P_D$	1	W
DC Output Current	$I_{OUT}$	50	mA
Soldering Temperature (under 10 sec)	$T_{solder}$	260	°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

**TRUTH TABLE**

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	$I_{SB}$ , $I_{SB1}$
Output Disable	L	H	H	High - Z	$I_{CC}$
Read	L	L	H	$D_{OUT}$	$I_{CC}$
Write	L	X	L	$D_{IN}$	$I_{CC}$

Note: H =  $V_{IH}$ , L =  $V_{IL}$ , X = Don't care.

**DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	$V_{IH}$		2.2	$V_{CC} + 0.5$	V	
Input Low Voltage	$V_{IL}$		-0.5	0.8	V	
Input Leakage Current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq V_{CC}$	-1	1	$\mu A$	
Output Leakage Current	$I_{LO}$	$V_{SS} \leq V_{I/O} \leq V_{CC}$ $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	-1	1	$\mu A$	
Output High Voltage	$V_{OH}$	$I_{OH} = -4mA$	2.4	-	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 8mA$	-	0.4	V	
Operating Power Supply Current	$I_{CC}$	$\overline{CE} = V_{IL}$ , $I_{I/O} = 0mA$ , Cycle=Min.	-8	-	190	mA
			-10	-	180	mA
			-12	-	160	mA
			-15	-	140	mA
Standby Power Supply Current	$I_{SB}$	$\overline{CE} = V_{IH}$	-	30	mA	
	$I_{SB1}$	$\overline{CE} \geq V_{CC} - 0.2V$	-	5	mA	

**CAPACITANCE** (TA=25°C, f=1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C <sub>IN</sub>	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

**AC TEST CONDITIONS**

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 30pF, I <sub>OH</sub> /I <sub>OL</sub> = -4mA/8mA

**AC ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5V±10%, TA = 0°C to 70°C)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t <sub>RC</sub>	8	-	10	-	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t <sub>ACE</sub>	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t <sub>OE</sub>	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t <sub>CLZ*</sub>	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t <sub>OLZ*</sub>	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t <sub>CHZ*</sub>	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t <sub>OHZ*</sub>	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	3	-	ns

**(2) WRITE CYCLE**

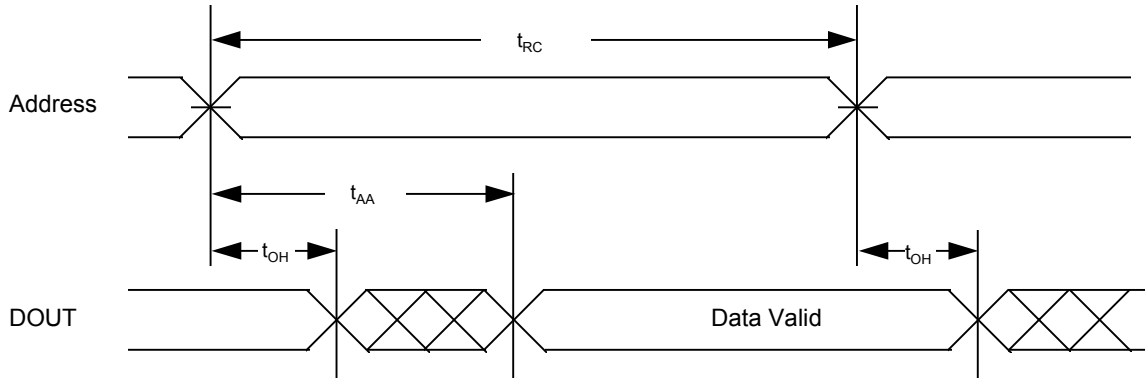
PARAMETER	SYMBOL	UT61256-8		UT61256-10		UT61256-12		UT61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t <sub>WC</sub>	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t <sub>AW</sub>	6.5	-	8	-	12	-	15	-	ns
Chip Enable to End of Write	t <sub>CW</sub>	6.5	-	8	-	12	-	15	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t <sub>WP</sub>	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t <sub>DW</sub>	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t <sub>DH</sub>	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t <sub>OW*</sub>	1.5	-	2	-	3	-	4	-	ns
Write to Output in High Z	t <sub>WHZ*</sub>	-	5	-	6	-	7	-	8	ns

\*These parameters are guaranteed by device characterization, but not production tested.

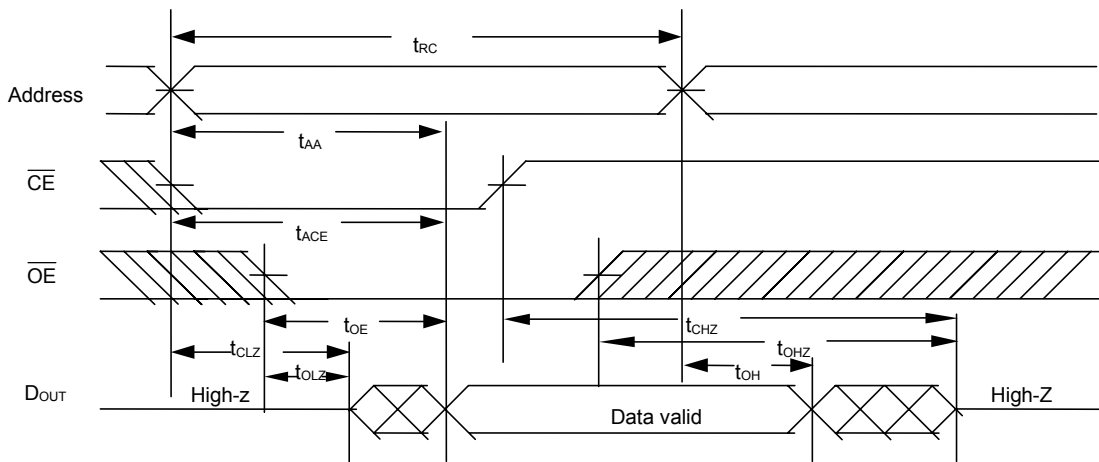


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 ( $\overline{CE}$  and  $\overline{OE}$  Controlled) (1,3,5,6)

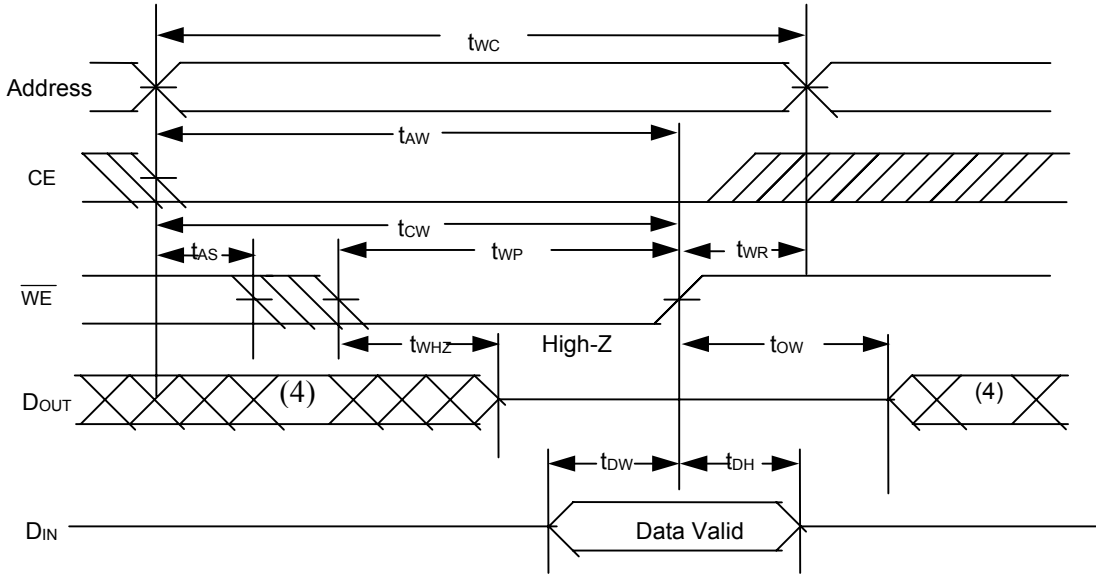


Notes :

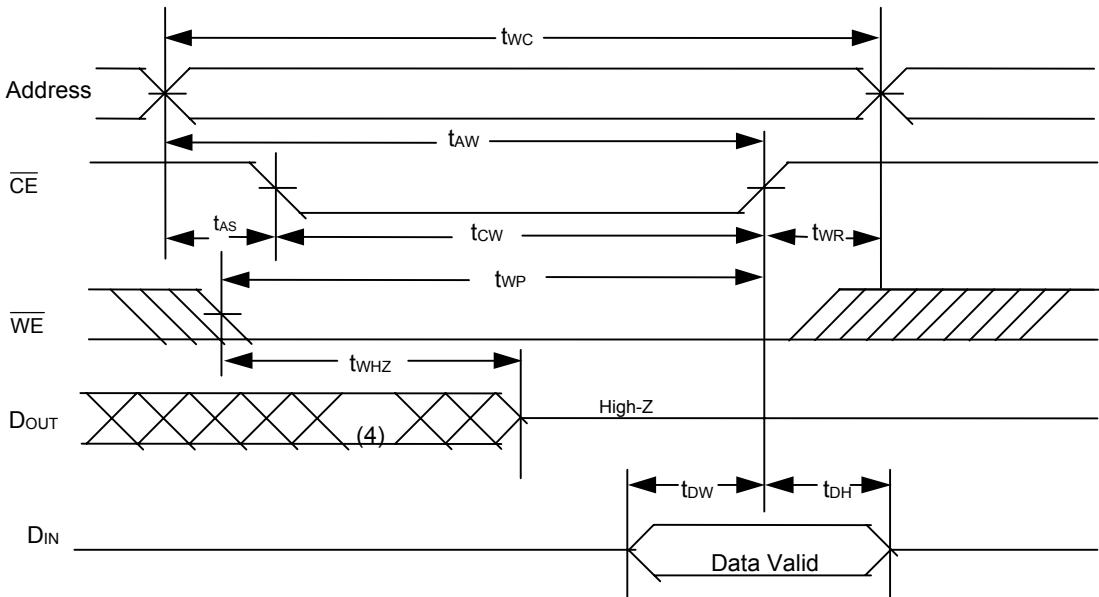
1.  $\overline{WE}$  is HIGH for read cycle.
2. Device is continuously selected  $\overline{CE} = V_{IL}$ .
3. Address must be valid prior to or coincident with  $\overline{CE}$  transition; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is LOW.
5.  $t_{CLZ}$ ,  $t_{OLZ}$ ,  $t_{CHZ}$  and  $t_{OHZ}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.
6. At any given temperature and voltage condition,  $t_{CHZ}$  is less than  $t_{CLZ}$ ,  $t_{OHZ}$  is less than  $t_{OLZ}$ .



**WRITE CYCLE 1 ( $\overline{WE}$  Controlled) (1,2,3,5)**



**WRITE CYCLE 2 ( $\overline{CE}$  Controlled) (1,2,5)**



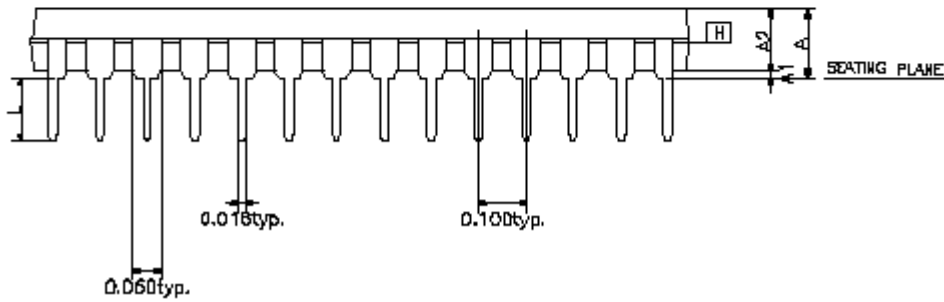
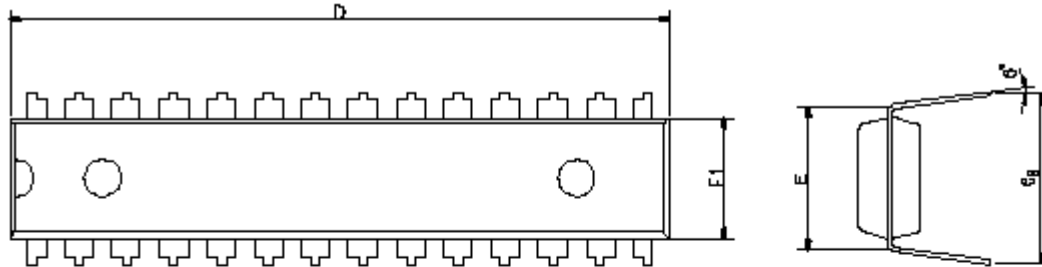
Notes :

1.  $\overline{WE}$  or  $\overline{CE}$  must be HIGH during all address transitions.
2. A write occurs during the overlap of a low  $\overline{CE}$  and a low  $\overline{WE}$ .
3. During a  $\overline{WE}$  controlled with write cycle with  $\overline{OE}$  LOW,  $t_{pw}$  must be greater than  $t_{whz}+t_{dw}$  to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CE}$  LOW transition occurs simultaneously with or after  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.
6.  $t_{ow}$  and  $t_{whz}$  are specified with  $C_L = 5pF$ . Transition is measured  $\pm 500mV$  from steady state.



PACKAGE OUTLINE DIMENSION

28 pin 300 mil skinny PDIP Package Outline Dimension



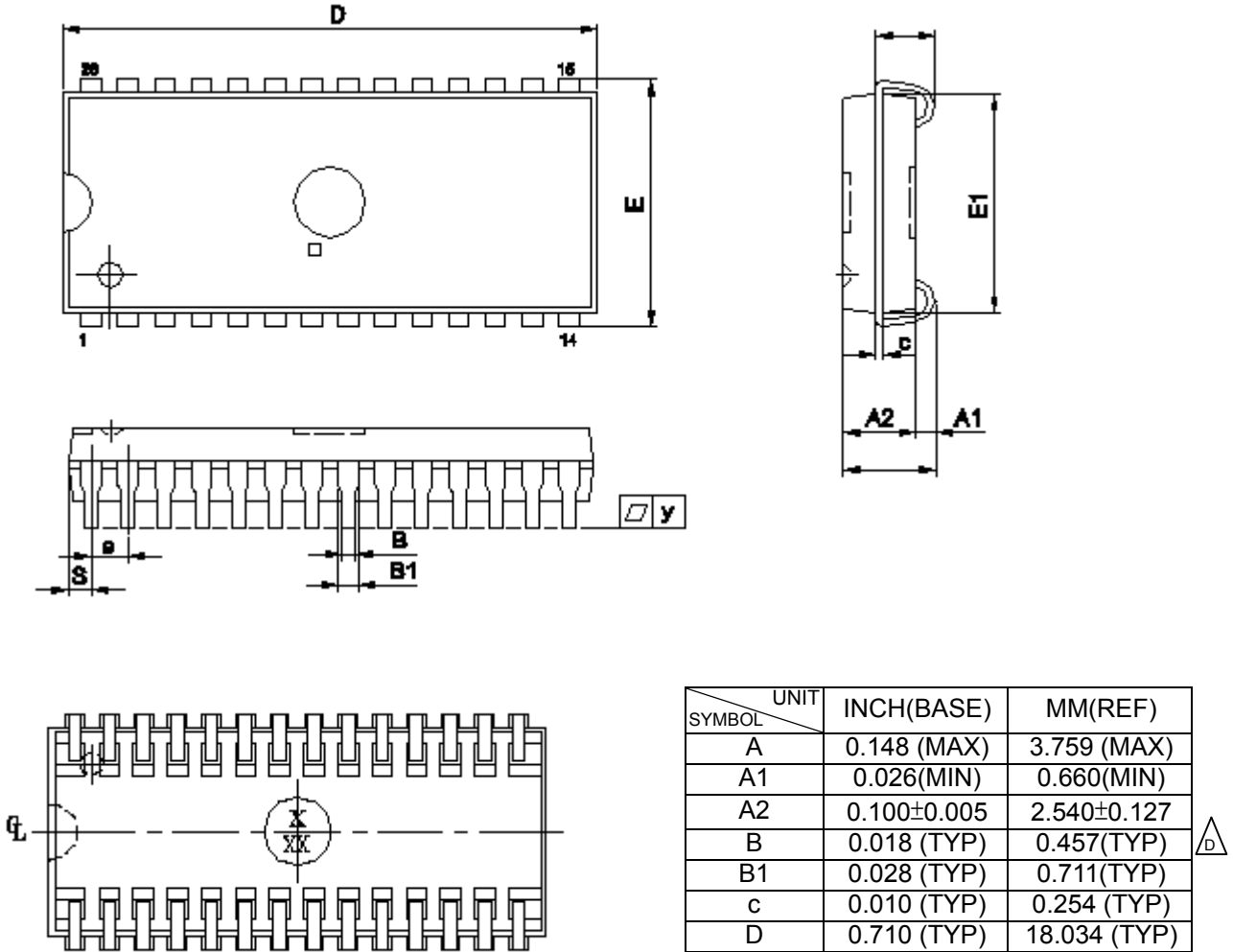
SYMBOL	UNIT	MIN	NOR.	MAX
A		-	-	0.210
A1		0.015	-	-
A2		0.125	0.130	0.135
D		1.385	1.390	1.400
E		0.310 BSC		
E1		0.283	0.288	0.293
L		0.115	0.130	0.150
eB		0.330	0.350	0.370
$\theta^\circ$		0	7	15

Note :

1. JEDEC OUTLINE : N / A



28pin 300 mil SOJ Package Outline Dimension

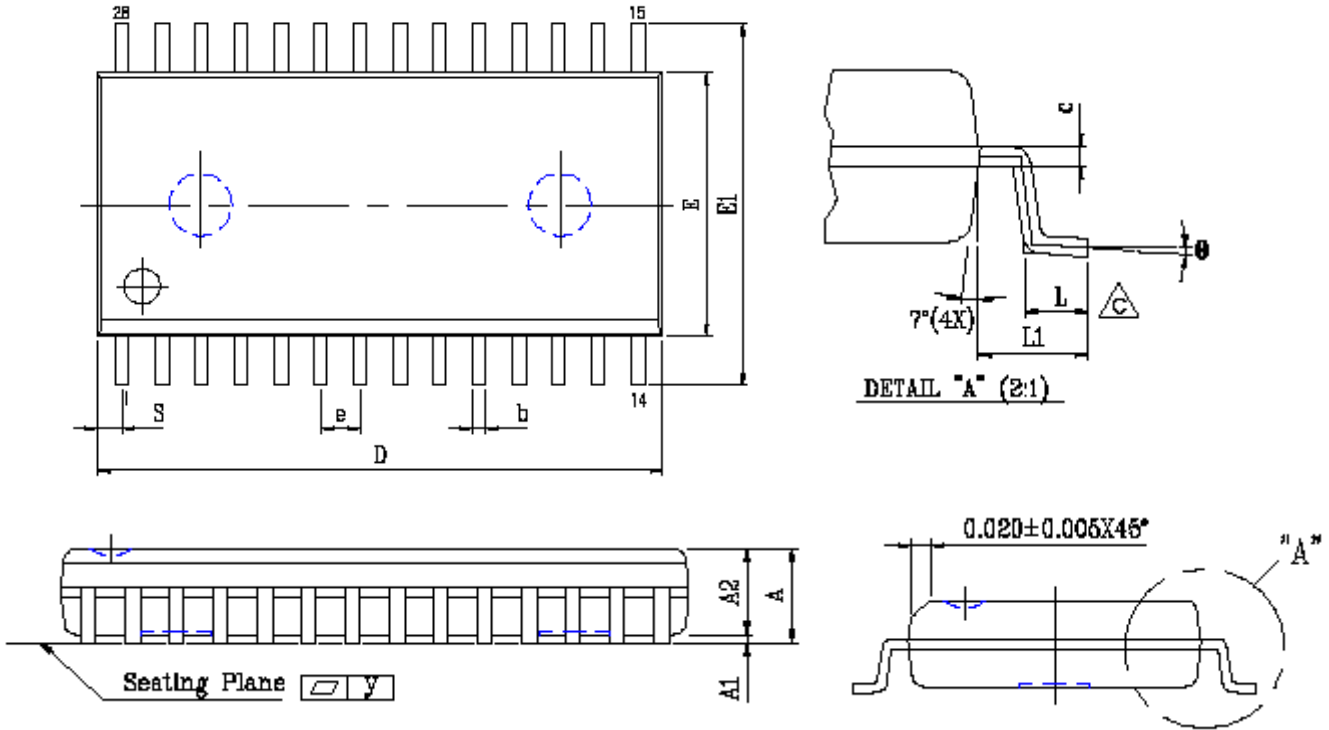


SYMBOL \ UNIT	INCH(BASE)	MM(REF)
A	0.148 (MAX)	3.759 (MAX)
A1	0.026(MIN)	0.660(MIN)
A2	0.100±0.005	2.540±0.127
B	0.018 (TYP)	0.457(TYP)
B1	0.028 (TYP)	0.711(TYP)
c	0.010 (TYP)	0.254 (TYP)
D	0.710 (TYP)	18.034 (TYP)
E	0.335(TYP)	8.509(TYP)
E1	0.3 (TYP)	7.620(TYP)
e	0.050 (TYP)	1.270 (TYP)
L	0.087±0.010	2.210±0.254
S	0.030 (TYP)	0.762 (TYP)
Y	0.003(MAX)	0.076(MAX)

- Note:
1. S/E/D DIM. NOT INCLUDING MOLD FLASH.
  2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THAN 10 MILS EACH SIDE.



28 pin 330 mil SOP Package Outline Dimension

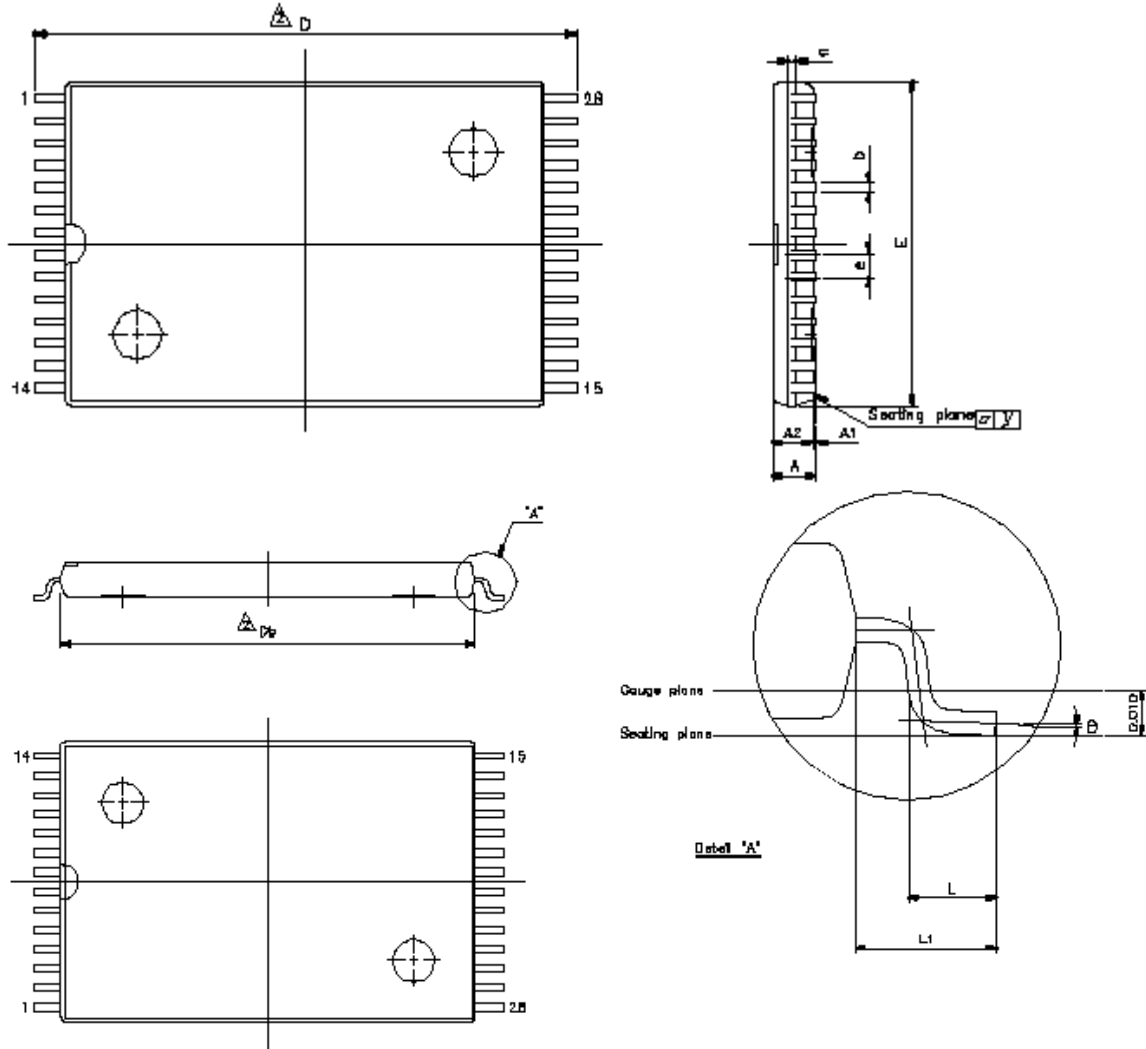


SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.120 (MAX)	3.048 (MAX)
A1		0.002(MIN)	0.05(MIN)
A2		0.098±0.005	2.489±0.127
b		0.016 (TYP)	0.406(TYP)
c		0.010 (TYP)	0.254(TYP)
D		0.728 (MAX)	18.491 (MAX)
E		0.350 (MAX)	8.890 (MAX)
E1		0.465±0.012	11.811±0.305
e		0.050 (TYP)	1.270(TYP)
L		0.05 (MAX)	1.270 (MAX)
L1		0.067±0.008	1.702±0.203
S		0.047 (MAX)	1.194 (MAX)
y		0.003(MAX)	0.076(MAX)
θ		0°~10°	0°~10°





28 pin 8x13.4mm STSOP Package Outline Dimension



Note :  
E dimension is not including end flash  
The total of both sides' end flash is  
Not above 0.3mm.

SYMBOL	UNIT	INCH(BASE)	MM(REF)
A		0.047 (MAX)	1.20 (MAX)
A1		0.004±0.002	0.10±0.05
A2		0.039±0.002	1.00±0.05
b		0.006 (TYP)	0.15(TYP)
c		0.010 (TYP)	0.254(TYP)
△ Db		0.465±0.004	11.80±0.10
E		0.315±0.004	8.00±0.10
e		0.022 (TYP)	0.55(TYP)
△ D		0.528±0.008	13.40±0.20
△ L		0.020±0.004	0.50±0.10
△ L1		0.0315±0.004	0.80±0.10
△ y		0.08(MAX)	0.003(MAX)
θ		0°~5°	0°~5°



UTRON

Rev. 1.1

UT61256  
32K X 8 BIT HIGH SPEED CMOS SRAM

**ORDERING INFORMATION**

<b>PART NO.</b>	<b>ACCESS TIME (ns)</b>	<b>PACKAGE</b>
UT61256KC-15	15	28 PIN SKINNY PDIP
UT61256SC-15	15	28 PIN SOP
UT61256JC-8	8	28 PIN SOJ
UT61256JC-10	10	28 PIN SOJ
UT61256JC-12	12	28 PIN SOJ
UT61256JC-15	15	28 PIN SOJ
UT61256LS-8	8	28 PIN STSOP
UT61256LS-10	10	28 PIN STSOP
UT61256LS-12	12	28 PIN STSOP
UT61256LS-15	15	28 PIN STSOP



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### REVISION HISTORY

REVISION	DESCRIPTION	DATE
REV. 1.0	Original.	Sep, 2000
REV 1.1	1. The package name of TSOP-1 is revised as STSOP. 2. The symbols CE#, OE# and WE# are revised as $\overline{CE}$ , $\overline{OE}$ and $\overline{WE}$ 3. Add part number in ordering information.	May 15, 2001



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