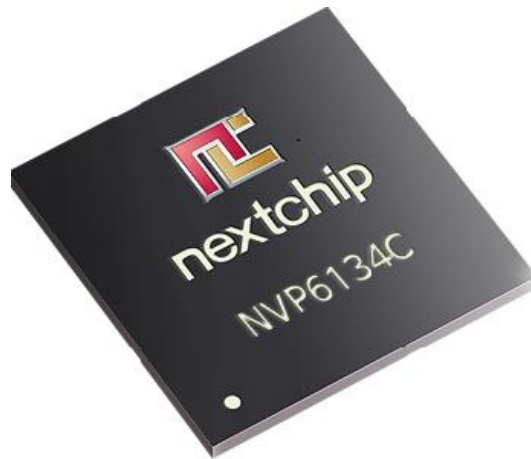


# NVP6134C

## Datasheet

**4-CH Universal RX(up to 5M NRT) and 5-CH Audio Codec**

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# REVISION HISTORY

NVP6134C Data sheet

| Rev.    | Date.      | Description          | Note |
|---------|------------|----------------------|------|
| REV 0.0 | 2016-06-08 | Initial Draft        | -    |
| REV 1.0 | 2016-10-12 | Adding AHD 4M/5M NRT | -    |
|         |            |                      | -    |
|         |            |                      | -    |
|         |            |                      | -    |
|         |            |                      | -    |

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## Product Overview

**NVP6134C** includes Universal 4-Channel RX and 5-Channel Audio Codec. It delivers high quality CVBS, 1M, 2M and 3/4/5M NRT image. It accepts separate CVBS, COMET, Universal 1M, 2M and 3/4/5M NRT inputs from Camera and the other video signal sources. It digitizes and decodes CVBS, COMET, Universal 1M/2M and 3/4/5M NRT Analog video signal into digital video components which represents 8-bit BT.656/BT.1120 4:2:2 byte interleave format with 74.25, 148.5 and 297MHz multiplexed.

**NVP6134C** includes Clock PLL, so each output byte interleave function available. Especially, It is able to use same transmission cable with conventional one for COMET(SD level), 1M(HD level), 2M(FHD level) and 3/4/5M NRT, and they provide the superior-image quality by minimizing the interference when separating Y and C.

5-Channel Audio Codec is 4-Channel Voice/1-Channel Mic PCM Codec which handles voice band signals(300Hz~3400Hz) with 8bit/16bit linear PCM, 8bit G.711(u-law, a-law) PCM. Built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

4-Channel Universal Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable.

## Features

### 1. Video Decoder

#### ● Input Formats

- 4CH Video Input
- : CVBS / COMET
- : Universal 1M, 2M and 3/4/5M NRT

#### ● Output Formats

- Output in BT.656/BT.1120 4:2:2 byte interleave format with 37.125/74.25/148.5/297MHz
- Support Sync Separate BT.601 Format (CLK/ H,V-SYNC/ 8'bit DATA)

#### ● Image Signal Processor

- Support Video Standard Auto-Detection up to 5M NRT for Each CH
- Support 2\*Video Output Port, Each Port Video Output Format Selectable
- On Chip Analog CLAMP/Anti-aliasing Filter and EQ Filter
- Accepts CVBS, COMET, 720P@25p/30p/50p/60p, 1080P@25p/30p, 1536P@18p, 1440@15p, 1944@12.5p
- Robust Sync detection for weak and unstable signals
- High-performance adaptive comb filter and Notch Filter
- Programmable H/V Peaking filter for Luminance
- CTI (Chrominance Transient Improvement)
- Color compensation for PAL
- IF compensation filter
- Robust No-video detection
- Programmable Brightness, Contrast, Saturation and Hue
- Programmable Picture Quality Control
- Programmable Gamma Correction

### 2. Audio Codec

- 4-Ch Voice / 1-Ch Mic Record, 1-Ch Playback
- 10bit pipe-line ADC / 1\*DAC
- In/output Analog PGA Control
- Linear PCM (8bit/16bit, 8K/16K/32K)
- G.711 a-law/u-law (8bits, 8K/16K/32K)
- Input Mixing, Digital Volume, Mute Detection
- SSP/DSP/I2S Interface (Master/Slave mode)
- Cascade mode (up to 4 cascade support)
- : 18-Channel recording (with 2 channel mic recording), mixing output, playback

### 3. MISC

- Built in Clock PLL
- Single 27M Oscillator for all video standards
- Built in 4-Ch Motion Detector(32x24)
- Support Coaxial Protocols for All Video Standard
- Support Each Channel MPP Pin and IRQ Pin
- Support I2C serial Interface

### 4. Operating Voltage

- 3.3V/1.2V Supply Voltage

### 5. Power Consumption

- T.B.D.

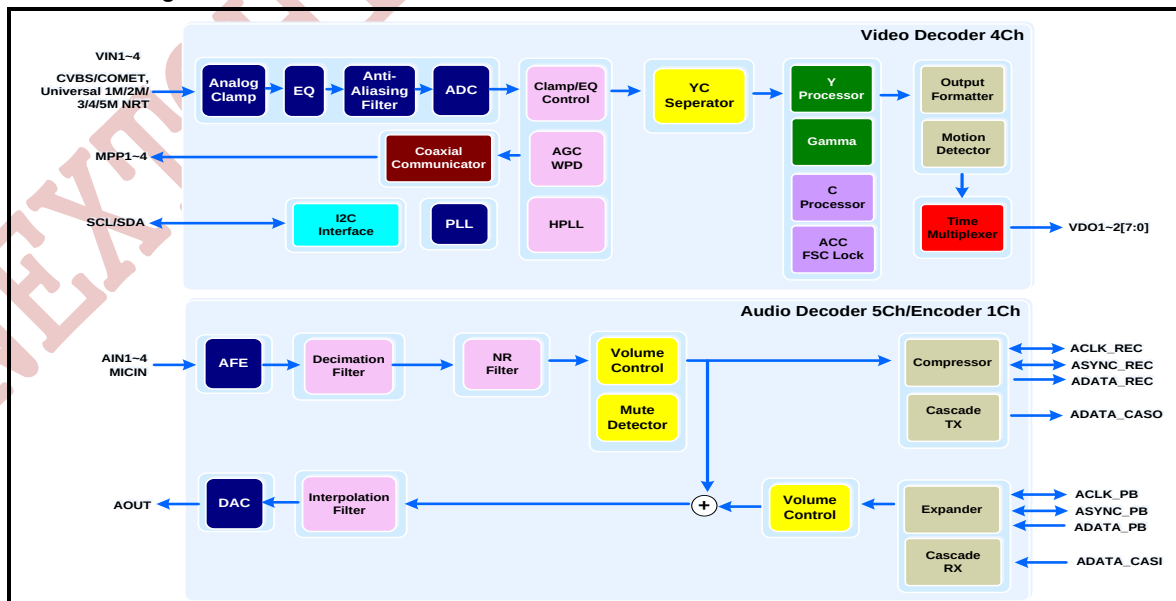
### 6. Ordering information

| DEVICE   | PACKAGE | TEMPERATURE RANGE |
|----------|---------|-------------------|
| NVP6134C | 76e-QFN | 0 ~ 70 ℃          |

### 7. Related Products

- HI3520D-V300 / HI3521A / HI3531A

## Functional block diagram



# TABLE OF CONTENTS

|                                                                                  |           |
|----------------------------------------------------------------------------------|-----------|
| Revision History .....                                                           | 2         |
| Table of Contents .....                                                          | 4         |
| Contents of Tables .....                                                         | 6         |
| Contents of Figures .....                                                        | 7         |
| <b>Chapter 1 PIN INFORMATION .....</b>                                           | <b>8</b>  |
| 1.1 PIN ASSIGNMENTS .....                                                        | 8         |
| 1.2 PIN DESCRIPTION .....                                                        | 9         |
| <b>Chapter 2 UNIVERSAL RX(1M,2M, and 3/4/5M_NRT) .....</b>                       | <b>11</b> |
| 2.1 FUNCTIONAL OVERVIEW .....                                                    | 11        |
| 2.2 VIDEO INPUT FORMATS .....                                                    | 12        |
| 2.3 ANALOG FRONT END (CLAMP, ANTI-ALIASING FILTER, EQ FILTER) .....              | 13        |
| 2.4 GENLOCK (ROBUST SYNC DETECTION, ROBUST NO-VIDEO DETECTION) .....             | 13        |
| 2.5 YCS (Y/C SEPARATOR) .....                                                    | 14        |
| 2.6 LUMA PROCESSING .....                                                        | 14        |
| 2.7 CHROMA PROCESSING .....                                                      | 14        |
| 2.8 DATA OUTPUT ORDER & DIRECTION CONTROL .....                                  | 16        |
| 2.9 OUTPUT FORMAT .....                                                          | 17        |
| 2.9.1 ITU-R BT.656/BT.1120 FORMAT .....                                          | 17        |
| 2.9.2 ITU-R BT.601 FORMAT .....                                                  | 17        |
| 2.9.3 VIDEO OUTPUT TIMING INFORMATION .....                                      | 18        |
| 2.10 OUTPUT MODE .....                                                           | 20        |
| 2.10.1 SINGLE OUTPUT MODE .....                                                  | 20        |
| 2.10.2 2-MULTIPLEX OUTPUT MODE .....                                             | 21        |
| 2.10.3 4-MULTIPLEX OUTPUT MODE .....                                             | 22        |
| 2.11 297MHz INTERFACE AND MULTI STANDARD OUTPUT MODE .....                       | 25        |
| 2.12 Video Frame Control .....                                                   | 25        |
| 2.13 MOTION DETECTOR .....                                                       | 26        |
| <b>Chapter 3 AUDIO CODEC .....</b>                                               | <b>27</b> |
| 3.1 Record Output .....                                                          | 27        |
| 3.1.1 Data Output Interface .....                                                | 28        |
| 3.1.2 2/4/8/16-Channels Data Output(256 fs) .....                                | 29        |
| 3.1.3 2/4/8/16-Channels Audio Data Output with 4-Channels Mic Data(320 fs) ..... | 30        |
| 3.1.4 ADATA_SP Output .....                                                      | 31        |
| 3.2 Playback Output .....                                                        | 32        |
| 3.3 Audio Detection .....                                                        | 32        |
| 3.4 Cascade Operation .....                                                      | 32        |
| <b>Chapter 4 COAXIAL PROTOCOL .....</b>                                          | <b>33</b> |
| 4.1 PELCO PROTOCOL .....                                                         | 33        |
| 4.2 A-CP(AHD-Coaxial protocol) .....                                             | 34        |
| <b>Chapter 5 I2C INTERFACE .....</b>                                             | <b>36</b> |
| <b>Chapter 6 REGISTER DESCRIPTION .....</b>                                      | <b>37</b> |
| 6.1 REGISTER ADDRESS .....                                                       | 37        |
| 6.1.1 BANK0 Register(0x00~0x1F) : VIDEO .....                                    | 37        |
| 6.1.2 BANK0 Register(0x20~0x3F) : VIDEO .....                                    | 38        |
| 6.1.3 BANK0 Register(0x40~0x5F) : VIDEO .....                                    | 39        |
| 6.1.4 BANK0 Register(0x60~0x7F) : VIDEO .....                                    | 40        |
| 6.1.5 BANK0 Register(0x80~0xA3) : VIDEO_ENABLE & Delay .....                     | 41        |
| 6.1.6 BANK0 Register(0xA8~0xF5) : STATUS .....                                   | 42        |
| 6.1.7 BANK1 Register(0x00~0x1E) : AUDIO .....                                    | 43        |
| 6.1.8 BANK1 Register(0x20~0x44) : AUDIO .....                                    | 44        |
| 6.1.9 BANK1 Register(0x80~0x9F) : IP Power Down .....                            | 45        |
| 6.1.10 BANK1 Register(0xB0~0xBF) : MPP .....                                     | 45        |
| 6.1.11 BANK1 Register(0xC2~0xCE) : OUTPUT PORT .....                             | 45        |
| 6.1.12 BANK2 Register(0x00~0x1F) : MOTION .....                                  | 46        |
| 6.1.13 BANK3~4 Register(0x00~0x7F / 0x80~0xFF) : COAXIAL .....                   | 47        |
| 6.1.14 BANK3~4 Register(0x00~0x1F / 0x80~0x9F) : COAXIAL CH1~4 .....             | 48        |

|                   |                                                          |           |
|-------------------|----------------------------------------------------------|-----------|
| 6.1.15            | BANK3~4 Register(0x20~0x5D / 0xA0~0xDD ) : COAXIAL CH1~4 | 49        |
| 6.1.16            | BANK3~4 Register(0x60~0x7F / 0xE0~0xFF ) : COAXIAL CH1~4 | 50        |
| 6.2               | Register Detail Description                              | 51        |
| 6.2.1             | VIDEO Registers                                          | 51        |
| 6.2.2             | Enable Registers                                         | 60        |
| 6.2.3             | State Registers                                          | 62        |
| 6.2.4             | AUDIO Registers                                          | 67        |
| 6.2.5             | Power Down Registers                                     | 76        |
| 6.2.6             | MPP Control Registers                                    | 77        |
| 6.2.7             | Video Output Control Registers                           | 78        |
| 6.2.8             | MOTION Registers                                         | 80        |
| 6.2.9             | COAXIAL Registers                                        | 81        |
| <b>Chapter 7</b>  | <b>Guide Note</b>                                        | <b>87</b> |
| 7.1               | Video Format Setting Register                            | 87        |
| 7.2               | Each Format FSC Setting Register                         | 87        |
| 7.3               | When Auto Detection, Video Format Classifier             | 88        |
| 7.4               | Coaxial Setting Register                                 | 88        |
| <b>Chapter 8</b>  | <b>ELECTRICAL CHARACTERISTICS</b>                        | <b>89</b> |
| 8.1               | ABSOLUTE MAXIMUM RATINGS                                 | 89        |
| 8.2               | RECOMMENDED OPERATING CONDITION                          | 89        |
| 8.3               | DC CHARACTERISTICS                                       | 89        |
| 8.4               | AC CHARACTERISTICS                                       | 90        |
| <b>Chapter 9</b>  | <b>AUDIO SYSTEM APPLICATIONS</b>                         | <b>91</b> |
| 9.1               | AUDIO 4-Channel Mode                                     | 91        |
| 9.2               | AUDIO 8-Channel Mode                                     | 91        |
| 9.3               | AUDIO 16-Channel Mode                                    | 92        |
| <b>Chapter 10</b> | <b>PACKAGE INFORMATION</b>                               | <b>93</b> |

# Contents of Tables

|                                                                 |    |
|-----------------------------------------------------------------|----|
| Table 1.1 NVP6134C PIN Description .....                        | 10 |
| Table 2.1 NVP6134C INPUT VIDEO IMAGE FORMATS .....              | 12 |
| Table 2.2 Data Output Pin Order Control .....                   | 16 |
| Table 2.3 Output Clock and Data Direction Control .....         | 16 |
| Table 2.4 1Port 1-Channel Normal mode or X-Format Setting ..... | 20 |
| Table 2.5 1Port 2-Channel Normal mode or X-Format Setting ..... | 21 |
| Table 2.6 1Port 4-Channel Normal mode or X-Format Setting ..... | 22 |
| Table 3.1 Sampling & PCM coding setting .....                   | 27 |
| Table 3.2 Record Output Interface configuration .....           | 28 |

# CONTENTS OF FIGURES

|                                                                                                 |    |
|-------------------------------------------------------------------------------------------------|----|
| Figure 1.1 Pin Assignments .....                                                                | 8  |
| Figure 2.1 Universal RX Video Processing of NVP6134C.....                                       | 11 |
| Figure 2.2 Anti-aliasing Filter characteristic .....                                            | 13 |
| Figure 2.3 Band Split Filter Characteristic .....                                               | 14 |
| Figure 2.4 Peaking Filter Characteristic .....                                                  | 14 |
| Figure 2.5 Chroma Process .....                                                                 | 15 |
| Figure 2.6 Chroma Low Pass filter Characteristic.....                                           | 15 |
| Figure 2.7 Region of active is constant .....                                                   | 17 |
| Figure 2.8 BT.601 Interface .....                                                               | 17 |
| Figure 2.9 AHD720P@30P/25P, 60P/50P Horizontal Timing Diagram.....                              | 18 |
| Figure 2.10 AHD720P@30P/25P, 60P/50P Vertical Timing Diagram .....                              | 18 |
| Figure 2.11 AHD1080P@30P/25P Horizontal Timing Diagram .....                                    | 19 |
| Figure 2.12 AHD1080P@30P/25P Vertical Timing Diagram .....                                      | 19 |
| Figure 2.13 Block Diagram of Single-Channel Output .....                                        | 20 |
| Figure 2.14 Block Diagram of of Multiplexed 2-Channels Output.....                              | 21 |
| Figure 2.15 Block Diagram of Multiplexed 4-Channels Output.....                                 | 22 |
| Figure 2.16 NVP6134C generate 297MHz(1Port 4-CH) data output.....                               | 23 |
| Figure 2.17 NVP6134C Select Channel ID .....                                                    | 23 |
| Figure 2.18 Method for Control Video Frame .....                                                | 25 |
| Figure 2.19 Motion Block Mapping.....                                                           | 26 |
| Figure 3.1 Timing of I2S mode .....                                                             | 28 |
| Figure 3.2 Timing of DSP mode .....                                                             | 28 |
| Figure 3.3 Timing of SSP mode .....                                                             | 29 |
| Figure 3.4 audio 2/4/8/16 channels data output <I2S mode, 256fs> .....                          | 29 |
| Figure 3.5 audio 2/4/8/16channels data output <DSP/SSP mode, 256fs>.....                        | 29 |
| Figure 3.6 audio 2/4/8/16 channels data output(with 2 channels mic) <I2S mode, 320fs> .....     | 30 |
| Figure 3.7 audio 2/4/8/16 channels data output(with 2 channels mic) <DSP/SSP mode, 320fs> ..... | 30 |
| Figure 3.8 ADATA_SP Output <I2S mode> .....                                                     | 31 |
| Figure 3.9 ADATA_SP Output <DSP/SSP mode> .....                                                 | 31 |
| Figure 3.10 Consist of Cascade System using 4-NVP6134C.....                                     | 32 |
| Figure 4.1 Coaxitron Active line .....                                                          | 33 |
| Figure 4.2 Description of One Coaxitron Bit .....                                               | 33 |
| Figure 4.3 Coaxitron Bit Timing.....                                                            | 33 |
| Figure 4.4 Data Structure of Coaxitron Origins (VBI 18th) .....                                 | 34 |
| Figure 4.5 A-CP Active line .....                                                               | 34 |
| Figure 4.6 Description of A-CP One Data Bit.....                                                | 35 |
| Figure 4.7 Data A-CP Bit Timing.....                                                            | 35 |
| Figure 4.8 Data Structure of Coaxitron Origins (VBI 17th) .....                                 | 35 |
| Figure 5.1 I2C Timing Diagram .....                                                             | 36 |
| Figure 5.2 I2C Slave Address Configuration.....                                                 | 36 |
| Figure 8.1 SCL and SDA Timing Diagram.....                                                      | 90 |
| Figure 9.1 AUDIO 4-channel Mode .....                                                           | 91 |
| Figure 9.2 AUDIO 8-channel Mode .....                                                           | 91 |
| Figure 9.3 AUDIO 16-channel Mode .....                                                          | 92 |
| Figure 10.1 NVP6134C 76Pin Package Information .....                                            | 93 |

# Chapter 1

## PIN INFORMATION

### 1.1 PIN ASSIGNMENTS

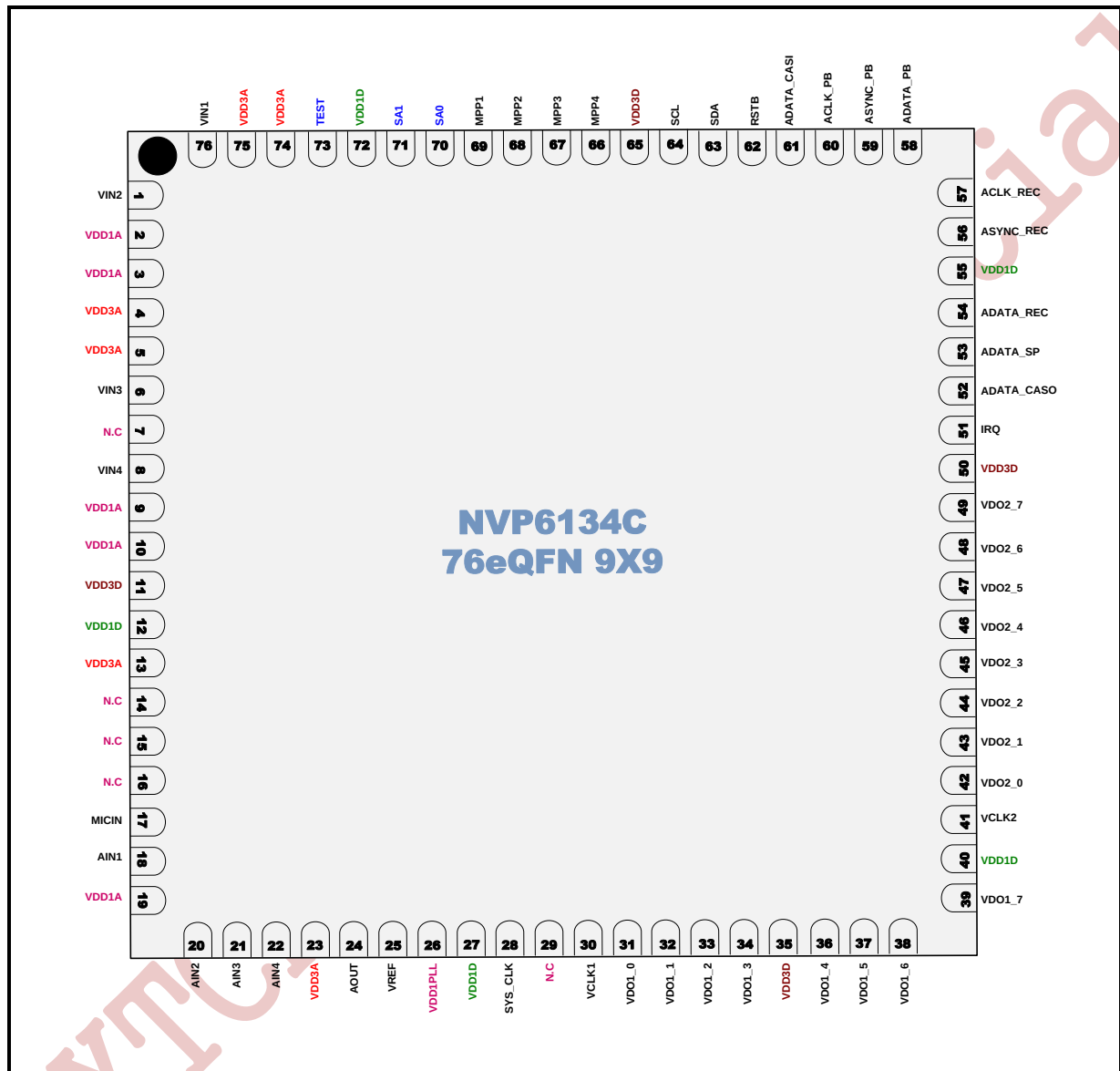


Figure 1.1 Pin Assignments



## 1.2 PIN DESCRIPTION

| Module Name             |    |                                                           |         |
|-------------------------|----|-----------------------------------------------------------|---------|
| NAME                    | IO | DESCRIPTION                                               | PIN NO. |
| System Service          |    |                                                           |         |
| RSTB                    | DI | System Reset(Active Low)                                  | 62      |
| SYS_CLK                 | DI | Oscillator Input (27MHz)                                  | 28      |
| TEST                    | I  | Chip Test mode selection PIN (Normally Connect to Ground) | 73      |
| Analog Input Interface  |    |                                                           |         |
| VIN1                    | AI | Analog Video Input 1                                      | 76      |
| VIN2                    | AI | Analog Video Input 2                                      | 1       |
| VIN3                    | AI | Analog Video Input 3                                      | 6       |
| VIN4                    | AI | Analog Video Input 4                                      | 8       |
| AIN1                    | AI | Analog Audio Input1                                       | 18      |
| AIN2                    | AI | Analog Audio Input2                                       | 20      |
| AIN3                    | AI | Analog Audio Input3                                       | 21      |
| AIN4                    | AI | Analog Audio Input4                                       | 22      |
| MICIN                   | AI | Analog Mic Input                                          | 17      |
| ETC                     |    |                                                           |         |
| IRQ                     | O  | Interrupt Request Output                                  | 51      |
| ACLK_REC                | B  | Clock for Record (M:output, S:Input)                      | 57      |
| ASYNCR_REC              | B  | Sync for Record(M:output, S:Input)                        | 56      |
| ADATA_REC               | O  | Audio Digital Data for Record                             | 54      |
| ADATA_SP                | O  | Audio Digital Data for Speaker                            | 53      |
| ADATA_CASO              | O  | Audio Digital Data for Cascade Output                     | 52      |
| ADATA_CASI              | I  | Audio Digital Data for Cascade Input                      | 61      |
| ACLK_PB                 | B  | Clock for Playback (M:output, S:Input)                    | 60      |
| ASYNCR_PB               | B  | Sync for Playback (M:output, S:Input)                     | 59      |
| ADATA_PB                | I  | Audio Digital Data for Playback                           | 58      |
| MPP1                    | O  | Coaxial Output1                                           | 69      |
| MPP2                    | O  | Coaxial Output2                                           | 68      |
| MPP3                    | O  | Coaxial Output3                                           | 67      |
| MPP4                    | O  | Coaxial Output4                                           | 66      |
| DIGITAL Video Interface |    |                                                           |         |
| VCLK1                   | O  | Video Output Clock1                                       | 30      |
| VDO1[7]                 | O  | Video Data Output 1[7]                                    | 39      |
| VDO1[6]                 | O  | Video Data Output 1[6]                                    | 38      |
| VDO1[5]                 | O  | Video Data Output 1[5]                                    | 37      |
| VDO1[4]                 | O  | Video Data Output 1[4]                                    | 36      |
| VDO1[3]                 | O  | Video Data Output 1[3]                                    | 34      |
| VDO1[2]                 | O  | Video Data Output 1[2]                                    | 33      |
| VDO1[1]                 | O  | Video Data Output 1[1]                                    | 32      |
| VDO1[0]                 | O  | Video Data Output 1[0]                                    | 31      |
| VCLK2                   | O  | Video Output Clock2                                       | 41      |
| VDO2[7]                 | O  | Video Data Output 2[7]                                    | 49      |
| VDO2[6]                 | O  | Video Data Output 2[6]                                    | 48      |
| VDO2[5]                 | O  | Video Data Output 2[5]                                    | 47      |
| VDO2[4]                 | O  | Video Data Output 2[4]                                    | 46      |
| VDO2[3]                 | O  | Video Data Output 2[3]                                    | 45      |
| VDO2[2]                 | O  | Video Data Output 2[2]                                    | 44      |
| VDO2[1]                 | O  | Video Data Output 2[1]                                    | 43      |
| VDO2[0]                 | O  | Video Data Output 2[0]                                    | 42      |

|                |    |                                        |                      |
|----------------|----|----------------------------------------|----------------------|
| AUDIO DAC      |    |                                        |                      |
| AOUT           | AO | Analog Audio Output                    | 24                   |
| VREF           | AO | Audio DAC Voltage Reference Output     | 25                   |
| I2C Interface  |    |                                        |                      |
| SCL            | I  | I2C Interface Clock (3.3V tolerant)    | 64                   |
| SDA            | B  | I2C Interface R/W Data (3.3V tolerant) | 63                   |
| SA0            | I  | Pin1 for Slave Address                 | 70                   |
| SA1            | I  | Pin2 for Slave Address                 | 71                   |
| Power          |    |                                        |                      |
| VDD1PLL        | P  | PLL Analog Power (1.2V)                | 26                   |
| VDD1D          | P  | Digital Power (Digital 1.2V)           | 12, 27, 40, 55, 72   |
| VDD3D          | P  | Digital Power (Digital 3.3V)           | 11, 35, 50, 65       |
| VDD1A          | P  | Analog Power (Analog 1.2V)             | 2, 3, 9, 10, 19      |
| VDD3A          | P  | Analog Power (Analog 3.3V)             | 4, 5, 13, 23, 74, 75 |
| No Connect Pin |    |                                        |                      |
| NC             | NC | Open                                   | 7, 14, 15, 16, 29    |
| Ground         |    |                                        |                      |
| PAD_GND        | G  | Exposed Pad                            | 77                   |

Table 1.1 NVP6134C PIN Description

# Chapter 2

## UNIVERSAL RX(1M,2M, and 3/4/5M\_NRT)

**NVP6134C** is a 4-Channel Universal RX which delivers high quality images. It accepts separate 4-Channel Universal Inputs from Camera and the other video signal sources.

It digitizes and decodes 4-Channel Universal 1M, 2M and 3/4/5M NRT video formats into digital component video which represents 8-bit ITU-R BT.656/1120 4:2:2 format and Sync Separate BT.601 Format with 27/36/37.125MHz, 54/72/74.25MHz and 108/144/148.5/297MHz multiplexed. 54/72/74.25/108/144/148.5/297MHz multiplex function is available, because it is in the range of Clock PLL.

**NVP6134C** includes 4-Channel analog processing circuit that comprises anti-aliasing filter, ADC, CLAMP and Equalizer filter. It shows the best image quality by adaptive high performance comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness, Contrast and several function such as CTI, Programmable peaking filter and various compensation filters.

### 2.1 FUNCTIONAL OVERVIEW

The Universal 1M, 2M and 3/4/5M NRT RX separates luminance and chrominance signals from Universal Inputs. Figure 2.1 show the block diagram of the **NVP6134C** video processing.

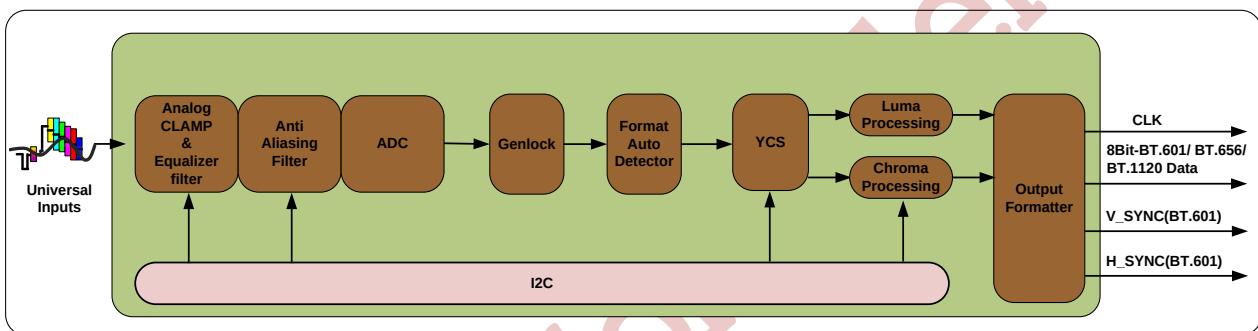


Figure 2.1 Universal RX Video Processing of NVP6134C

The First step to decode Universal RX is to digitize the entire video signal using an A/D converter (ADC). Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic. (AGC)

**NVP6134C** decides the attenuated image signal level via cable by EQ pattern; compensates the attenuated image signals by equalizer compensation filter. (EQ Pattern)

The video signal also is low-pass filtered in Anti aliasing Filter to remove any high-frequency components that may result in aliasing. Vertical sync and horizontal sync information are recovered in Genlock block.

In regard to various video formats, **NVP6134C** has the auto detection module for these video formats which uses different H/V Sync length according to each formats. (Video Standard Auto Detection)

When composite video signal is decoded, the luminance and chrominance are separated by YCS(Y/C Separator).

The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, Adaptive Comb Filter is used.

The color demodulator in chroma processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

## 2.2 VIDEO INPUT FORMATS

NVP6134C supports Universal Video Formats. Table 2.1 show various Video Formats and Register Setting Value (VIDEO\_FORMAT, 0x08~0B[4:0], Bank0/ AHD\_MD, 0x81~84[3:0], Bank0/ SPL\_MD, 0x85~89[3:0], Bank0 ) to support them.

| FORMAT        | HZ    | H x V              | Fsc(MHz)   | SPL_MD<br>( Bank0,<br>0x85~89[3:0] ) | AHD_MD<br>( Bank0,<br>0x81~84[3:0] ) | VIDEO_FORMAT<br>( Bank0,<br>0x08~0B[4:0] ) |
|---------------|-------|--------------------|------------|--------------------------------------|--------------------------------------|--------------------------------------------|
| NTSC-M,J      | 59.94 | 720x240<br>960x240 | 3.579545   | 0x0                                  | 0x0                                  | 0x00                                       |
| NTSC-4.43     | 59.94 | 720x240<br>960x240 | 4.43361875 |                                      |                                      | 0x11                                       |
| PAL-B,D,G,H,I | 50    | 720x288<br>960x288 | 4.43361875 |                                      |                                      | 0x1D                                       |
| PAL-M         | 59.94 | 720x240<br>960x240 | 3.57561149 |                                      |                                      | 0x16                                       |
| PAL-Nc        | 50    | 720x288<br>960x288 | 3.58205625 |                                      |                                      | 0x1F                                       |
| PAL-60        | 60    | 720x240<br>960x240 | 4.433619   |                                      |                                      | 0x15                                       |
| AHD_5M_12.5P  | 12.5  | 2592x1944          | Flexible   | 0x4                                  | 0x4                                  | Don't care                                 |
| AHD_4M_15P    | 15    | 2560x1440          | Flexible   |                                      |                                      |                                            |
| AHD_3M_18P    | 18    | 2048x1536          | Flexible   |                                      |                                      |                                            |
| AHD_1080_30   | 30    | 1920x1080          | Flexible   | 0x0                                  | 0x2                                  |                                            |
| AHD_1080_25   | 25    | 1920x1080          | Flexible   |                                      | 0x3                                  |                                            |
| AHD_720_60    | 60    | 1280x720           | Flexible   |                                      | 0x4                                  |                                            |
| AHD_720_50    | 50    | 1280x720           | Flexible   |                                      | 0x5                                  |                                            |
| AHD_720_30    | 30    | 1280x720           | Flexible   |                                      | 0x6                                  |                                            |
| AHD_720_25    | 25    | 1280x720           | Flexible   |                                      | 0x7                                  |                                            |

Table 2.1 NVP6134C INPUT VIDEO IMAGE FORMATS

## 2.3 ANALOG FRONT END (CLAMP, ANTI-ALIASING FILTER, EQ FILTER)

**NVP6134C** includes 4 Channel Analog Processing circuits that comprise anti-aliasing filter, EQ Filter, ADC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **NVP6134C**. Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register and include bypass mode that don't have AFE filtering.

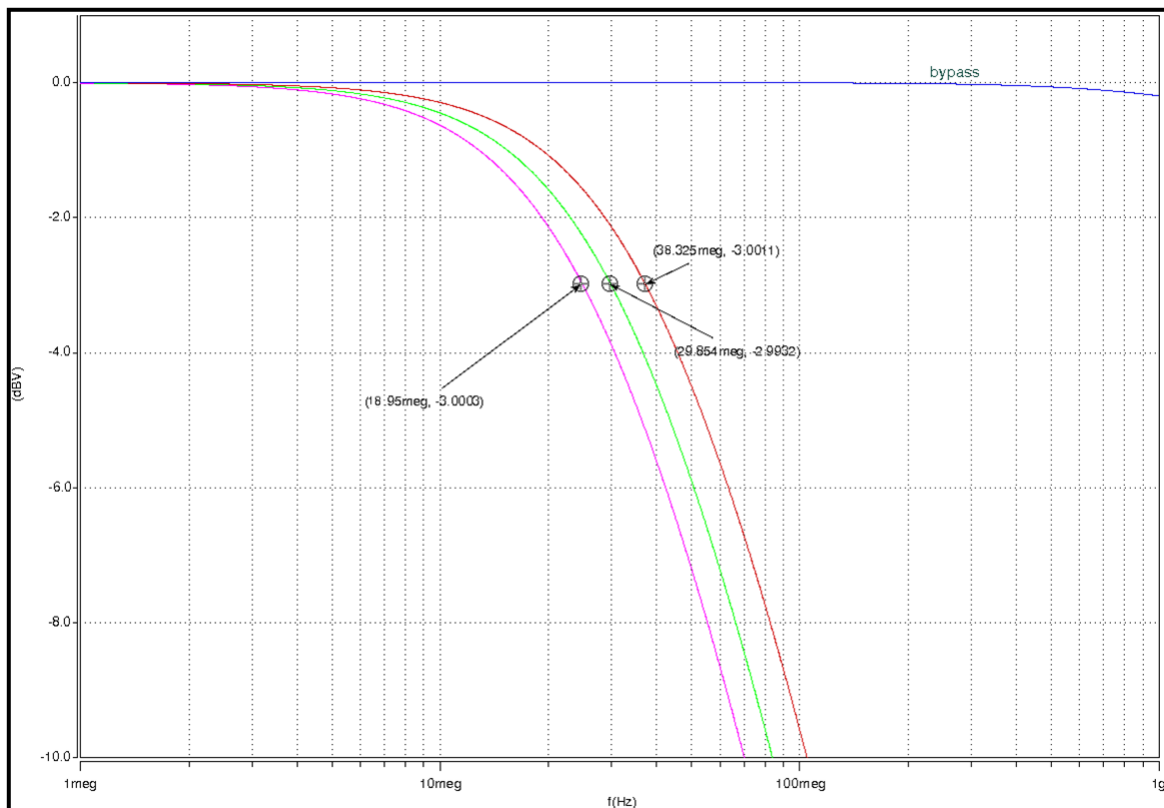


Figure 2.2 Anti-aliasing Filter characteristic

## 2.4 GENLOCK (ROBUST SYNC DETECTION, ROBUST NO-VIDEO DETECTION)

**NVP6134C** provides a fully digital Genlocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

**NVP6134C** uses the proprietary Genlock mechanism for video application system.

It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

## 2.5 YCS (Y/C SEPARATOR)

The YCS is used to separate Y and C signal from Universal standard video signal. Therefore, The output image is sharper and clearer compared to other device. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows partial Characteristic of BSF. According to Input signal format, BSF characteristic can be selected.

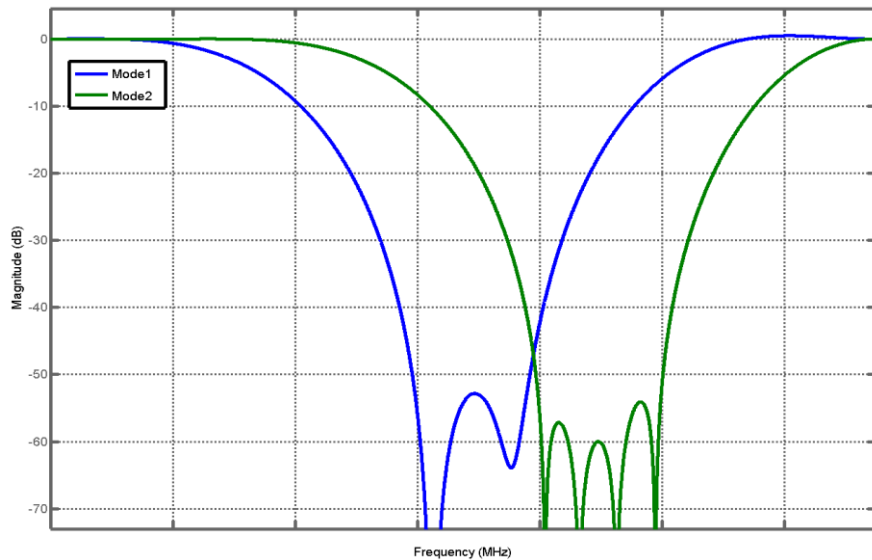


Figure 2.3 Band Split Filter Characteristic

**NVP6134C** can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **NVP6134C**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

## 2.6 LUMA PROCESSING

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

Figure 2.4. shows Peaking Filter Characteristic. **NVP6134C** provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y\_PEAK\_MODE, 0x18[7:4] / 0x19[7:4] / 0x1A[7:4] / 0x1B[7:4], Bank0) via I2C interface.

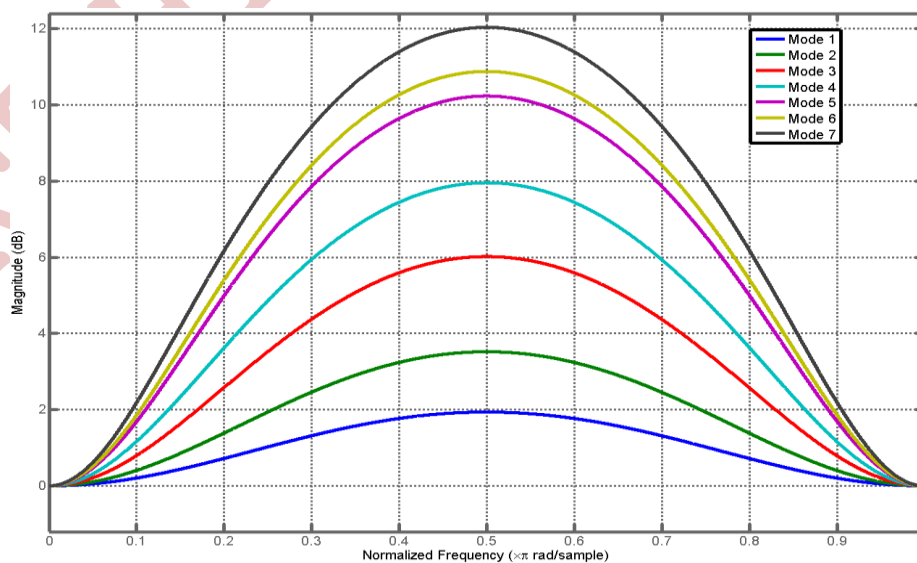


Figure 2.4 Peaking Filter Characteristic

## 2.7 CHROMA PROCESSING

The Chroma Processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The Chroma Demodulator receives modulated chroma from Y/C separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6.

Users can select the chroma filter through I2C interface (CLPF\_SEL, 0x21/25/29/2D[3:0], Bank0).

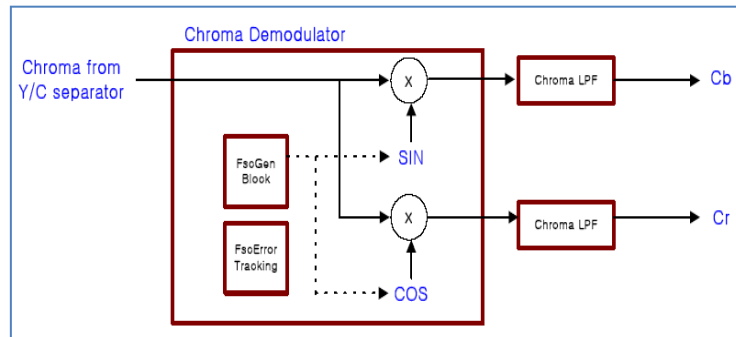


Figure 2.5 Chroma Process

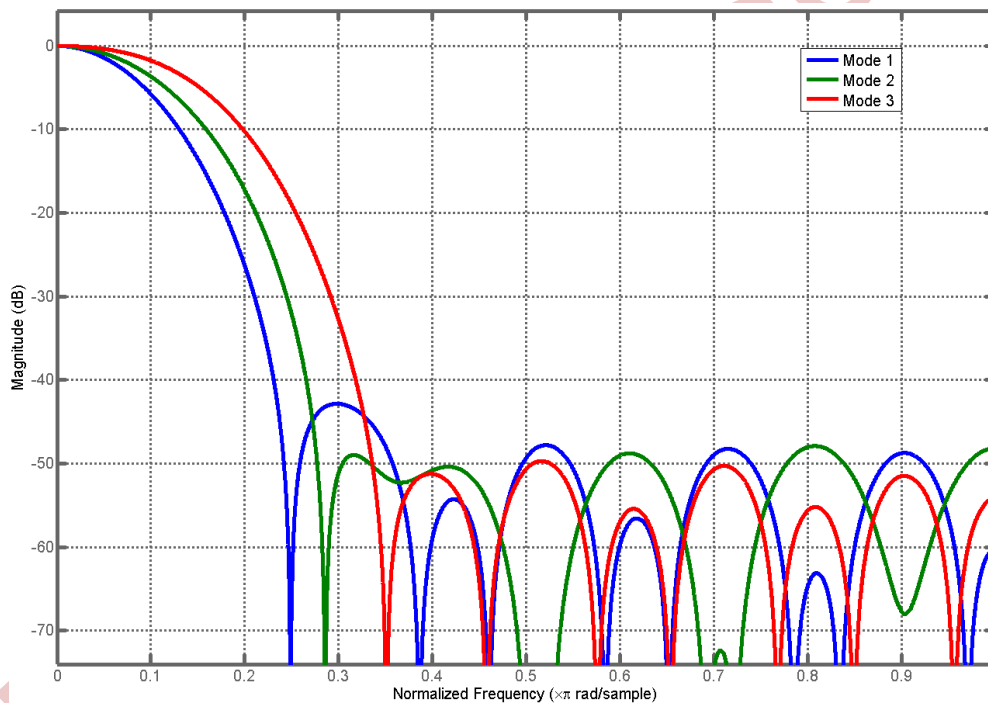


Figure 2.6 Chroma Low Pass filter Characteristic

## 2.8 DATA OUTPUT ORDER & DIRECTION CONTROL

**NVP6134C** can change the order of the output pin in the All Output Mode as shown in Table 2.2. (OUT\_DATA\_x\_INV, 0xCB[2:1] Bank1)  
Furthermore, as Clock and Data pins control direction so may it does nothing with interconnected back-end device and how control related control register as shown in Table 2.3. ( VCLK\_x\_EN, 0xCA[6:5] Bank1 / VDO\_x\_EN, 0xCA[2:1] Bank1 )

| Address (Bank1)         | state | Data Output of Port X |
|-------------------------|-------|-----------------------|
| 0xCB[1], OUT_DATA_1_INV | 0     | VDO_1 [7:0]           |
|                         | 1     | VDO_1 [0:7]           |
| 0xCB[2], OUT_DATA_2_INV | 0     | VDO_2 [7:0]           |
|                         | 1     | VDO_2 [0:7]           |

Table 2.2 Data Output Pin Order Control

| Address (Bank1)    | state | Data Output of Port X |
|--------------------|-------|-----------------------|
| 0xCA[5], VCLK_1_EN | 0     | HI-Z                  |
|                    | 1     | Output VCLK_1 Enable  |
| 0xCA[6], VCLK_2_EN | 0     | HI-Z                  |
|                    | 1     | Output VCLK_2 Enable  |
| 0xCA[1], VDO_1_EN  | 0     | HI-Z                  |
|                    | 1     | Output DATA1 Enable   |
| 0xCA[2], VDO_2_EN  | 0     | HI-Z                  |
|                    | 1     | Output DATA2 Enable   |

Table 2.3 Output Clock and Data Direction Control



## 2.9 OUTPUT FORMAT

NVP6134C supports a format of standard ITU-R BT.656/1120. Ports of 2 is synchronized by each output clock(VCLK\_A~VCLK\_B). Phase of clock is controlled by VCLK\_SEL(BANK1, 0xCD[7:4]/0xCE[7:4]) and VCLK\_DLY\_SEL(BANK1, 0xCD[3:0]/0xCE[3:0]).

### 2.9.1 ITU-R BT.656/BT.1120 FORMAT

Codes of SAV and EAV are injected into data stream of ITU-R BT.656/1120 to indicate a start and a end of active. Note that a number of pixel for 1H active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 2.7 shows data stream of ITU-R BT.656/1120 format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

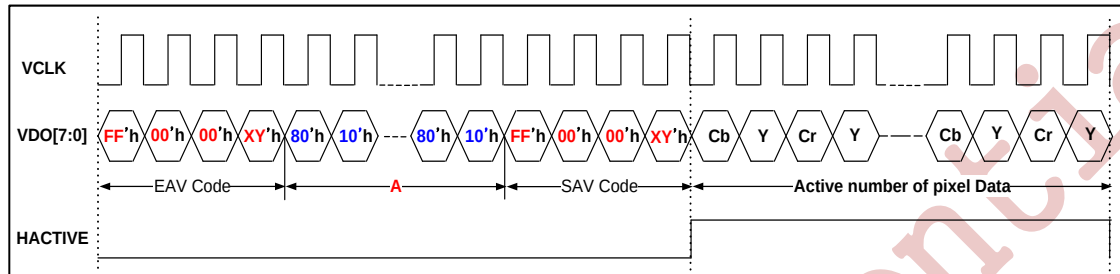


Figure 2.7 Region of active is constant

### 2.9.2 ITU-R BT.601 FORMAT

NVP6134C support a standard format of ITU-R BT.601. BT.601 Interface consist of 4 component, 8bit-Video Data, Video Clock, H-SYNC and V-Sync(Figure2.8). NVP6134C can output H/V-SYNC through MPP1~4 pin and Support up to AHD 1080@25/30P two channels.

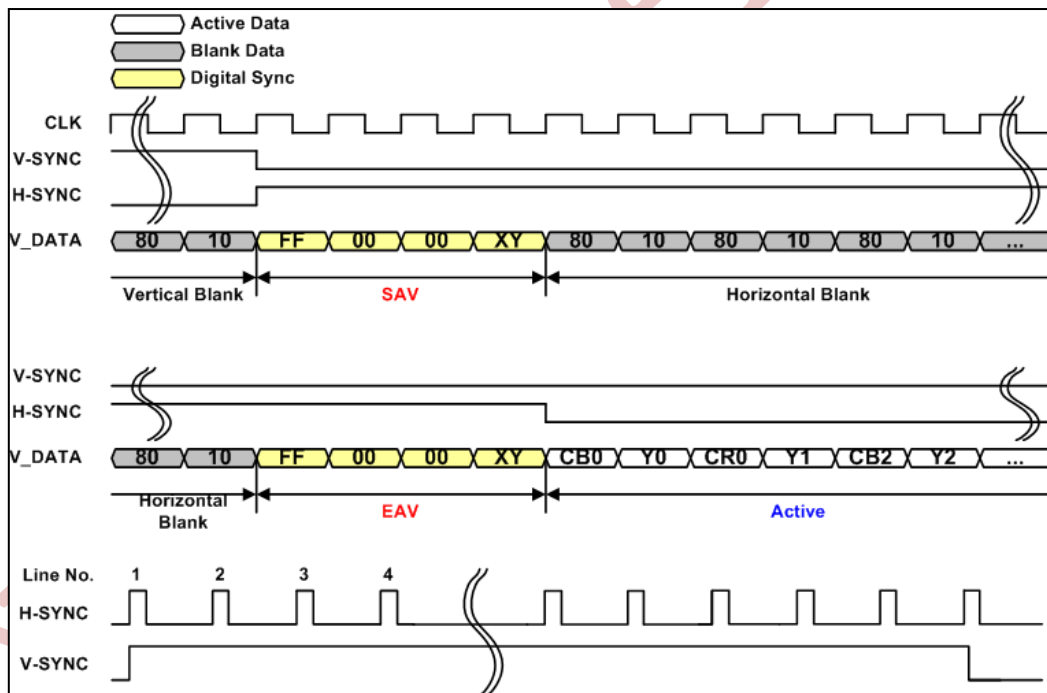


Figure 2.8 BT.601 Interface

### 2.9.3 VIDEO OUTPUT TIMING INFORMATION

The NVP6134C output timing is like with SD resolution. But some synchronous signals difference with SD resolution as Field information that does not separated EVEN/ODD field. There is next sentence shown timing diagram point of video output.

#### 2.9.3.1 AHD720P @ 30P/25P, 60P/50P H/V Timing

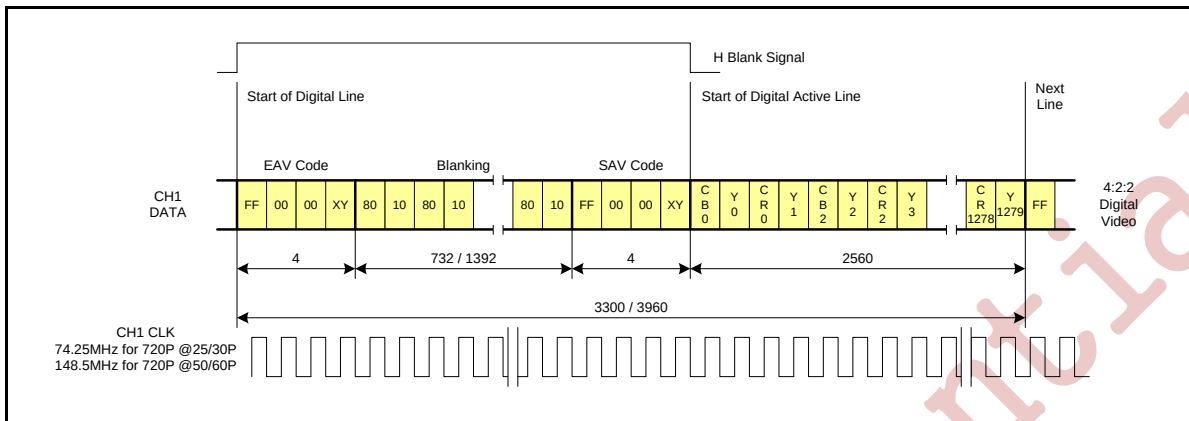


Figure 2.9 AHD720P@30P/25P, 60P/50P Horizontal Timing Diagram

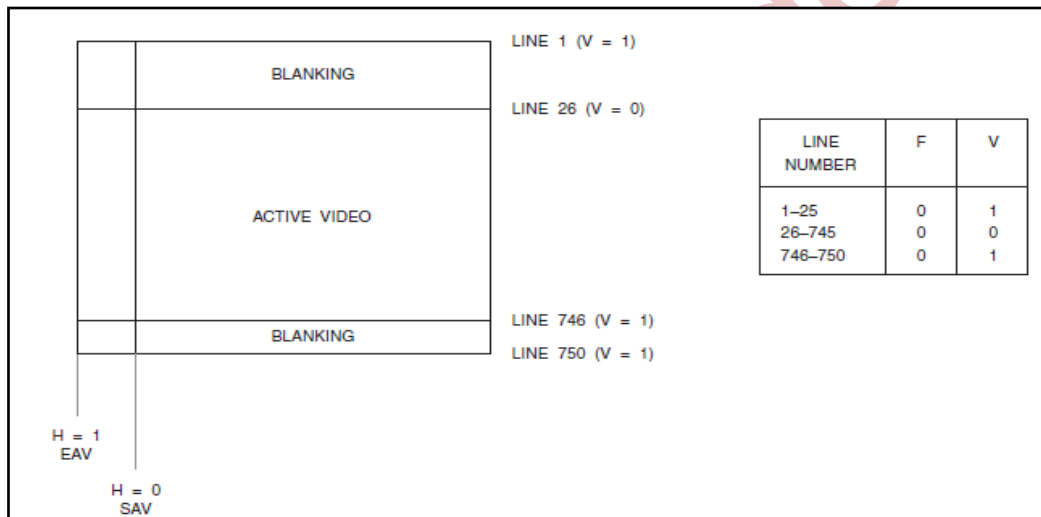


Figure 2.10 AHD720P@30P/25P, 60P/50P Vertical Timing Diagram

### 2.9.3.2 AHD1080P @ 30P/25P H/V Timing

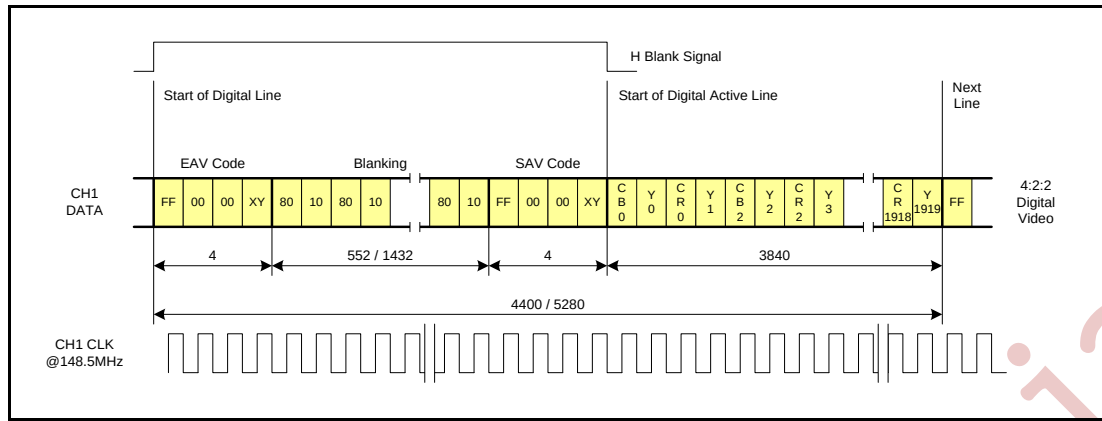


Figure 2.11 AHD1080P@30P/25P Horizontal Timing Diagram

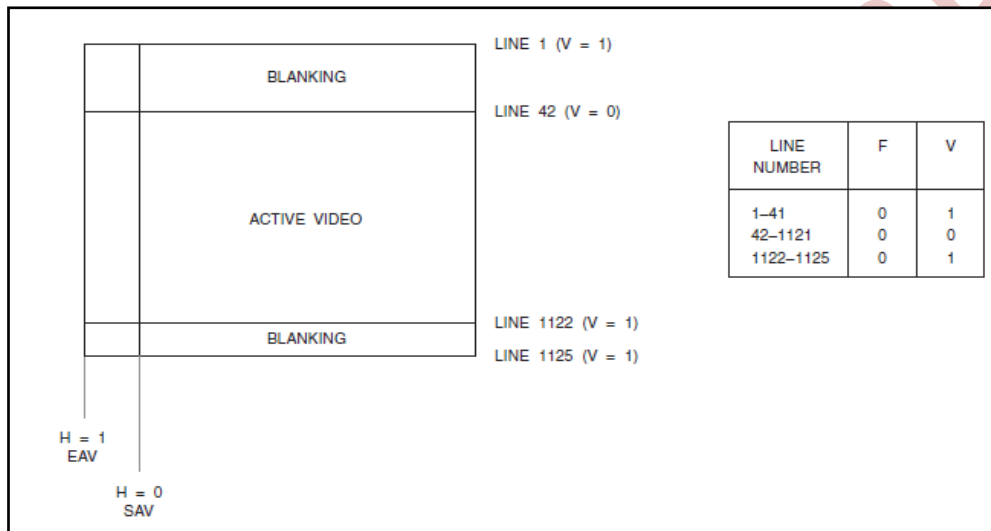


Figure 2.12 AHD1080P@30P/25P Vertical Timing Diagram

## 2.10 OUTPUT MODE

The NVP6134C output to the back-end devices whether transferring a channel by a port or 2/4-channels multiplexed output by a port. It is that as much as possible multiplexed channels by a port's output frequency same to sum of multiplexed video's frequency. The NVP6134C supports Variable Output Data Rate.

### 2.10.1 SINGLE OUTPUT MODE

Codes of SAV and EAV are injected into data stream of ITU-Basically, a video channel output through a port. **NVP6134C** output 2-clocks that VCLK1~2 and output 2-data that VDO1~2. There is timing as shown in Figure 2.13. For VCLK1~2 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Registers(Bank1 0xCD ~ CE).

| ADDRESS |      | REGISTER NAME      | BITS  | VALUE | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|------|--------------------|-------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                    |       |       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1       | 0xC2 | VPORT_1_SEQ1       | [3:0] | 0x0   | <b>VPORT_x_SEQy</b><br>: Select the type of output video signal through each video output port<br>(x = VDO output port number, y= channel count for 1-port)<br><br>0 : Normal Display of Channel 1      8 : H_half Display of Channel 1<br>1 : Normal Display of Channel 2      9 : H_half Display of Channel 2<br>2 : Normal Display of Channel 3      A : H_half Display of Channel 3<br>3 : Normal Display of Channel 4      B : H_half Display of Channel 4<br>Etc.: Don't use |
|         | 0xC4 | VPORT_2_SEQ1       | [3:0] | 0x1   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0xC8 | VPORT_1_CH_OUT_SEL | [7:4] | 0x0   | <b>VPORT_x_CH_OUT_SEL</b><br>: Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number)<br><br>0 : 1-Port 1CH data<br>2 : 1-Port 2CH time-mixed data<br>8 : 1-Port 4CH time-mixed data<br>Etc.: Don't use                                                                                                                                                                                                         |
|         | 0xC9 | VPORT_2_CH_OUT_SEL | [3:0] | 0x0   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

Table 2.4 1Port 1-Channel Normal mode or X-Format Setting

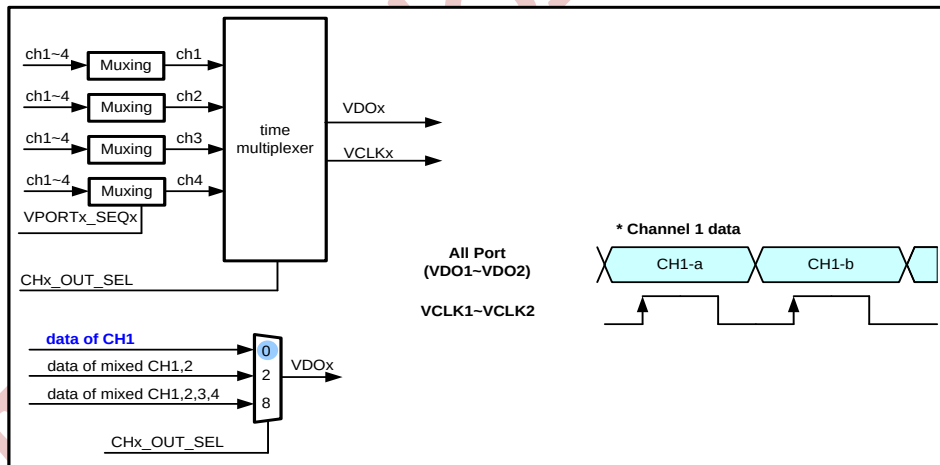


Figure 2.13 Block Diagram of Single-Channel Output

## 2.10.2 2-MULTIPLEX OUTPUT MODE

In the 2-Multiplex Output Mode, NVP6134C outputs multiplexed 2-channels video through one port. Also, NVP6134C supports the 1Port 2-Channel X-Format Mode. X-Format lowers the Horizontal Frequency in half.

1Port-2CH Normal or Horizontal half mode Setting Value is as below.(Table2. 5)

| ADDRESS |      | REGISTER NAME      | BITS  | VALUE       |        | DESCRIPTION                                                                                                                                                                                                                                                                                         |  |
|---------|------|--------------------|-------|-------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| Bank    | Addr |                    |       | Normal MODE | X MODE |                                                                                                                                                                                                                                                                                                     |  |
| 1       | 0xC2 | VPORT_1_SEQ1       | [3:0] | 0x10        | 0x98   | <b>VPORT_x_SEQy</b><br>: Select the type of output video signal through each video output port<br>(x = VDO output port number, y= channel count for 1-port)                                                                                                                                         |  |
|         |      | VPORT_1_SEQ2       | [7:4] |             |        |                                                                                                                                                                                                                                                                                                     |  |
|         | 0xC4 | VPORT_2_SEQ1       | [3:0] | 0x32        | 0xBA   | 0 : Nomal Display of Channel 1    8 : H_half Display of Channel 1<br>1 : Nomal Display of Channel 2    9 : H_half Display of Channel 2<br>2 : Nomal Display of Channel 3    A : H_half Display of Channel 3<br>3 : Nomal Display of Channel 4    B : H_half Display of Channel 4<br>Etc.: Don't use |  |
|         |      | VPORT_2_SEQ2       | [7:4] |             |        |                                                                                                                                                                                                                                                                                                     |  |
|         | 0xC8 | VPORT_1_CH_OUT_SEL | [7:4] | 0x2         |        | <b>VPORT_x_CH_OUT_SEL</b><br>: Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number)<br><br>0 : 1-Port 1CH data<br>2 : 1-Port 2CH time-mixed data<br>8 : 1-Port 4CH time-mixed data<br>Etc.: Don't use                          |  |
|         | 0xC9 | VPORT_2_CH_OUT_SEL | [3:0] |             |        |                                                                                                                                                                                                                                                                                                     |  |

Table 2.5 1Port 2-Channel Normal mode or X-Format Setting

Figure2.14 shown as multiplexed with 2-channels video output to VDO1~VDO2. For VCLK1~VCLK2 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register(Bank1 0xCD ~ CE).

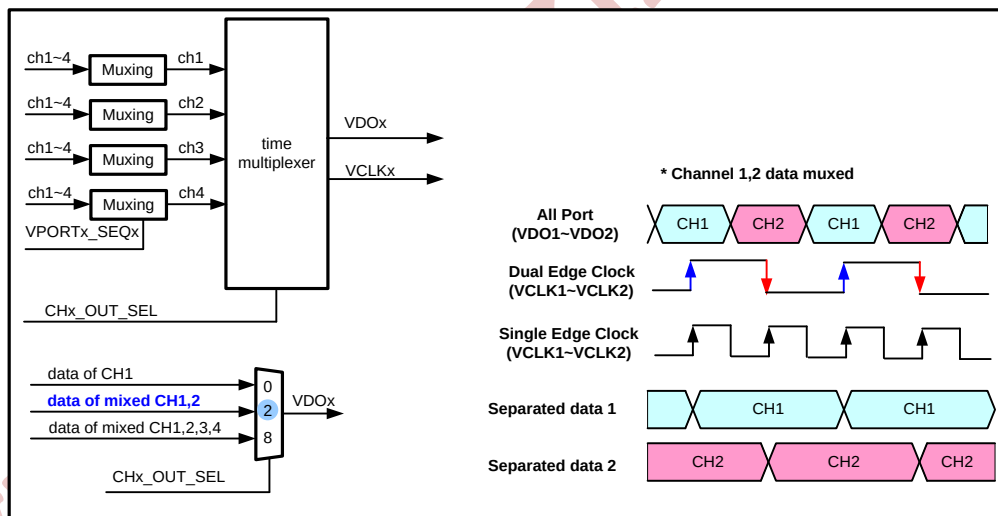


Figure 2.14 Block Diagram of Multiplexed 2-Channels Output

### 2.10.3 4-MULTIPLEX OUTPUT MODE

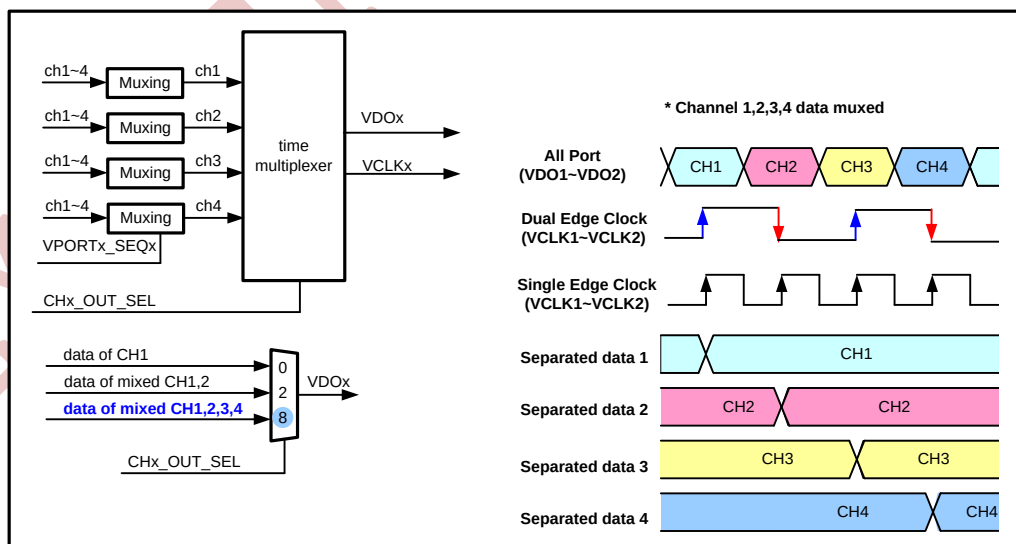
In the 4-Multiplex Output Mode, NVP6134C outputs multiplexed 4-channels video through one port. Also, NVP6134C supports the 1Port 4-Channels X-Format Mode. X-Format lowers the Horizontal Frequency in half.

1Port-4CH Normal or Horizontal half mode Setting Value is as below. (Table 2.6)

| Bank | Addr | REGISTER NAME      | BITS  | VALUE       |        | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|------|--------------------|-------|-------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |      |                    |       | Normal MODE | X MODE |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1    | 0xC2 | VPORT_1_SEQ1       | [3:0] | 0x10        | 0x98   | <b>VPORT_x_SEQy</b><br>: Select the type of output video signal through each video output port<br>(x = VDO output port number, y= channel count for 1-port)<br><br>0 : Nomal Display of Channel 1    8 : H_half Display of Channel 1<br>1 : Nomal Display of Channel 2    9 : H_half Display of Channel 2<br>2 : Nomal Display of Channel 3    A : H_half Display of Channel 3<br>3 : Nomal Display of Channel 4    B : H_half Display of Channel 4<br><br>Etc.: Don't use |
|      |      | VPORT_1_SEQ2       | [7:4] | 0x32        | 0xBA   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      | 0xC3 | VPORT_1_SEQ3       | [3:0] | 0x10        | 0x98   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |      | VPORT_1_SEQ4       | [7:4] | 0x32        | 0xBA   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      | 0xC4 | VPORT_2_SEQ1       | [3:0] | 0x10        | 0x98   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |      | VPORT_2_SEQ2       | [7:4] | 0x32        | 0xBA   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      | 0xC5 | VPORT_2_SEQ3       | [3:0] | 0x10        | 0x98   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      |      | VPORT_2_SEQ4       | [7:4] | 0x32        | 0xBA   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|      | 0xC8 | VPORT_1_CH_OUT_SEL | [3:0] | 0x8         |        | <b>VPORT_x_CH_OUT_SEL</b><br>: Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number)<br>0 : 1-Port 1CH data<br>2 : 1-Port 2CH time-mixed data<br>8 : 1-Port 4CH time-mixed data<br>Etc.: Don't use                                                                                                                                                                                                     |
|      | 0xC9 | VPORT_2_CH_OUT_SEL | [7:4] | 0x8         |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

Table 2.6 1Port 4-Channel Normal mode or X-Format Setting

NVP6134C support the 297MHz 1Port 4CH HD Data Out Mode. Four Channels HD data stream represents 8bit BT.656/1120 4:2:2 format with 297MHz multiplexed. Figure2.15 shown as multiplexed with 4-channels video output to VDO1~VDO2. For VCLK1~VCLK2 phase adjustment can be made against VDO1~VDO2 using "Clock Delay Control" Register.



■ Example of 297MHz 1Port 4-Channels Data Output Mode with Channel ID

1. In case of VDO1 output port and VCLK1 output clock use.
2. Set VDO1 output(CH\_OUT\_SEL1, BANK1, 0xC8[7:4] = 0x8) and VCLK1 output (VCLK1\_SEL, BANK1, 0xCD[7:4] = 0x4 or 0x5) .
3. Set Channel ID Type (Refer to CHID\_TYPE(Bank0, 0x54[2:0]) Register Description)
4. And then NVP6134C generate 297MHz(1Port 4CH) data output (Figure 2.16)

If you want to confirm the 297MHz Data using FPGA or Other device, Execute 5~11 item in next page.

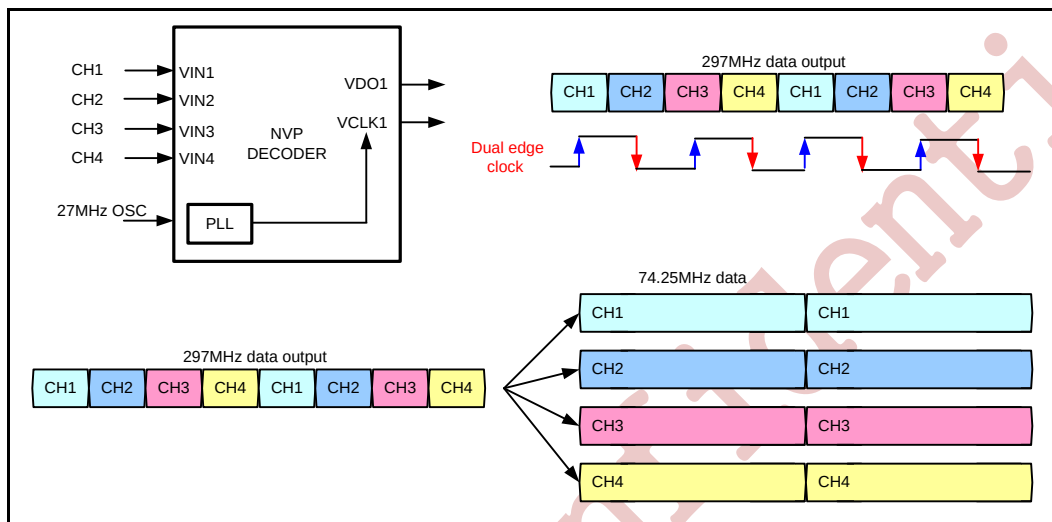


Figure 2.16 NVP6134C generate 297MHz(1Port 4-CH) data output

5. FPGA or equivalent devices which is input 297MHz time multiplexed data output, need to align with same channel data. (74.25MHz 1,2,3,4 channel). Figure2.17. shows how to use Channel ID as a example.

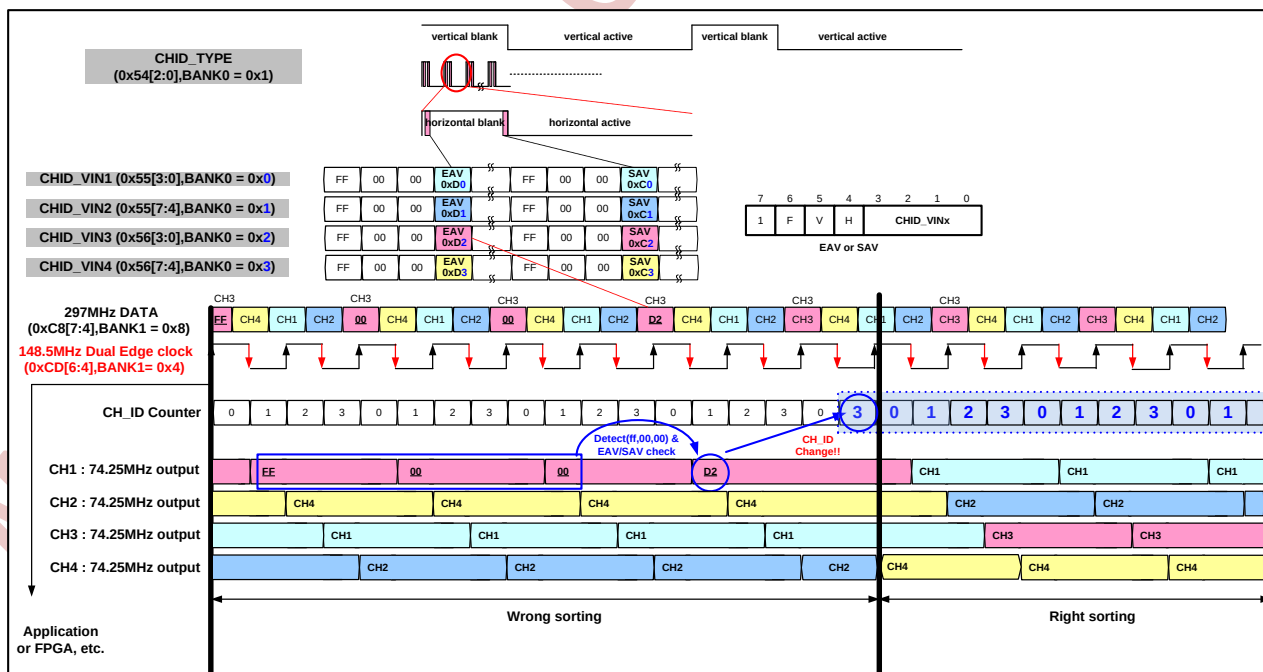


Figure 2.17 NVP6134C Select Channel ID

6. CHID\_TYPE(BANK0, 0x54[2:0]=001) mode described in top of Figure2.17.
7. To generate 2bit digit, Design 2bit counter with VCLK1 (The 2bit digit means each channel).
8. Using 2bit digit, Convert from 297MHz Data to 74.25MHz Data (Wrong sorting part in Figure2.17.) and then Define the 2bit digit ( 0 : Ch1 data, 1 : Ch2 data, 2 : Ch3 data, 3 : Ch4 data).  
namely, 297MHz data output separate only with 74.25MHz, 4channel data, is not align with channel data where becomes mapping in counter value.
9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel (1CH selected in Figure2.17.). If selected channel data become Right sorting condition, other 3 channel is sorted automatically.
10. Check the 1ch data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.
11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Figure2.17.)
12. Become Right sorting part.



## 2.11 297MHz INTERFACE AND MULTI STANDARD OUTPUT MODE

NVP6134C supports the frequency of output data up to 297MHz at maximum. Two Channel FHD data stream represents 8bit BT.656/1120 4:2:2 format with 297MHz multiplexed 1-port. Also, NVP6134C can output 2ch or 4ch signals with different standards(CVBS, 720p, 1080p, 3/4/5M\_NRT) through 1-port.

Available output combinations are as below.

- (1) 1-port 2-Channel combination
  - a. CVBS + 720P, CVBS + 720P, CVBS + 3M\_NRT
  - b. 720P + 1080P, 720P + 3M\_NRT
  - c. 1080P + 3M\_NRT
- (2) 1-port 4-Channel combination
  - a. CVBS 2CH + 720P 2CH
  - b. CVBS 2CH + 1080P\_X 2CH
  - c. CVBS + 720P + 1080P\_X 2CH
  - d. 720P 4CH
  - e. 1080P\_X 4CH

## 2.12 Video Frame Control

The **NVP6134C** supports that a frame control of video output. So it is function that the decoder's output masking by the EAV/SAV make to blank region. If set to FRM\_NRT\_ON is High, so output finally which set by FRM\_NRT\_SEQ[29:0] that each a bit of FRM\_NRT\_SEQ[29:0] match to each a frame. And the FRM\_NRT\_SEQ rotates continuous then to end from FRM\_NRT\_SEQ[0] to FRM\_NRT\_SEQ[29]. If the FRAME\_NRT\_SEQ bit set to Low, a apply frame has blank region. So, It received back-end device nothing to do because is not active region.

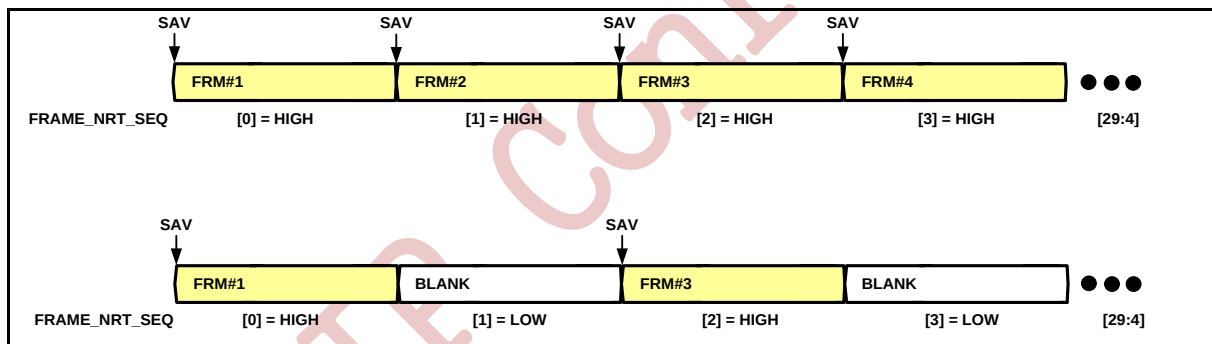


Figure 2.18 Method for Control Video Frame

## 2.13 MOTION DETECTOR

**NVP6134C** supports 4-Channels motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.19. to be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

|                                                                                                                                                      |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| <div> <div></div> : Motion Detection Information Block (16x12)         <div></div> : Motion Detection Internal Processing Block (32x24)       </div> |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 1                                                                                                                                                    | 2   | 3   | 4   | 5   | 6   | 7   | 8   | 9   | 10  | 11  | 12  | 13  | 14  | 15  | 16  |
| 17                                                                                                                                                   | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| 33                                                                                                                                                   | 34  | 35  | 36  | 37  | 38  | 39  | 40  | 41  | 42  | 43  | 44  | 45  | 46  | 47  | 48  |
| 49                                                                                                                                                   | 50  | 51  | 52  | 53  | 54  | 55  | 56  | 57  | 58  | 59  | 60  | 61  | 62  | 63  | 64  |
| 65                                                                                                                                                   | 66  | 67  | 68  | 69  | 70  | 71  | 72  | 73  | 74  | 75  | 76  | 77  | 78  | 79  | 80  |
| 81                                                                                                                                                   | 82  | 83  | 84  | 85  | 86  | 87  | 88  | 89  | 90  | 91  | 92  | 93  | 94  | 95  | 96  |
| 97                                                                                                                                                   | 98  | 99  | 100 | 101 | 102 | 103 | 104 | 105 | 106 | 107 | 108 | 109 | 110 | 111 | 112 |
| 113                                                                                                                                                  | 114 | 115 | 116 | 117 | 118 | 119 | 120 | 121 | 122 | 123 | 124 | 125 | 126 | 127 | 128 |
| 129                                                                                                                                                  | 130 | 131 | 132 | 133 | 134 | 135 | 136 | 137 | 138 | 139 | 140 | 141 | 142 | 143 | 144 |
| 145                                                                                                                                                  | 146 | 147 | 148 | 149 | 150 | 151 | 152 | 153 | 154 | 155 | 156 | 157 | 158 | 159 | 160 |
| 161                                                                                                                                                  | 162 | 163 | 164 | 165 | 166 | 167 | 168 | 169 | 170 | 171 | 172 | 173 | 174 | 175 | 176 |
| 177                                                                                                                                                  | 178 | 179 | 180 | 181 | 182 | 183 | 184 | 185 | 186 | 187 | 188 | 189 | 190 | 191 | 192 |

Figure 2.19 Motion Block Mapping

# Chapter 3

## AUDIO CODEC

**NVP6134C** outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. **NVP6134C** has 5 channels ADC and 1 channel DAC for audio signal.

Audio data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to **NVP6134C** via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

**NVP6134C** selects one audio input signal among 5 analog audio input(4-Ch Audio/1-Ch mic) and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 5 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, **NVP6134C** supports audio mute detection and cascade function up to 4 chips - audio 18 channels (16-Ch Audio/2-Ch mic)

### 3.1 Record Output

Analog audio data is converted to PCM data and this data is outputted to the other **NVP6134C** or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA\_REC pin used for data of each channel and ADATA\_SP pin used for one mixed signal of each channel's data. The output data from ADATA\_SP pin is either same data of ADATA\_REC pin or mixed signal of each channel's data.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law), unsigned linear PCM and linear PCM are supported. 8KHz / 16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

|                     | BANK1     |       |           |       |           |       |           |       |           |       |           |       |
|---------------------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|-----------|-------|
|                     | 8K/8bit   |       | 8K/16bit  |       | 16K/8bit  |       | 16K/16bit |       | 32K/8bit  |       | 32K/16bit |       |
|                     | ADDR      | VALUE | ADDR      | VALUE | ADDR      | VALUE | ADDR      | VALUE | ADDR      | VALUE | ADDR      | VALUE |
| Linear PCM          | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 1     | 0x00[0]   | 1     |
|                     | 0x07[3]   | 0     | 0x07[3]   | 0     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     |
|                     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     |
|                     | 0x08[5:4] | 00    | 0x08[5:4] | 00    | 0x08[5:4] | 00    | 0x08[5:4] | 00    | 0x08[5:4] | 00    | 0x08[5:4] | 00    |
| Unsigned Linear PCM | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 1     | 0x00[0]   | 1     |
|                     | 0x07[3]   | 0     | 0x07[3]   | 0     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     |
|                     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     |
|                     | 0x08[5:4] | 01    | 0x08[5:4] | 01    | 0x08[5:4] | 01    | 0x08[5:4] | 01    | 0x08[5:4] | 01    | 0x08[5:4] | 01    |
| G.711 U-law         | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 1     | 0x00[0]   | 1     |
|                     | 0x07[3]   | 0     | 0x07[3]   | 0     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     |
|                     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     |
|                     | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    |
| G.711 A-law         | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 1     | 0x00[0]   | 1     |
|                     | 0x07[3]   | 0     | 0x07[3]   | 0     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     |
|                     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     |
|                     | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    |
| G.711 A-law         | 0x08[6]   | 0     | 0x08[6]   | 0     | 0x08[6]   | 0     | 0x08[6]   | 0     | 0x08[6]   | 0     | 0x08[6]   | 0     |
|                     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 0     | 0x00[0]   | 1     | 0x00[0]   | 1     |
|                     | 0x07[3]   | 0     | 0x07[3]   | 0     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     | 0x07[3]   | 1     |
|                     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     | 0x07[2]   | 1     | 0x07[2]   | 0     |
| G.711 A-law         | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    | 0x08[5:4] | 10    |
|                     | 0x08[6]   | 1     | 0x08[6]   | 1     | 0x08[6]   | 1     | 0x08[6]   | 1     | 0x08[6]   | 1     | 0x08[6]   | 1     |

Table 3.1 Sampling & PCM coding setting

DSP / SSP / I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

### 3.1.1 Data Output Interface

**NVP6134C** outputs "Record Output" using ACLK\_REC, ASYNC\_REC, ADATA\_REC and DATA\_SP. ACLK\_REC is a reference clock signal for Record Output Data and ASYNC\_REC is a reference synchronization signal for Record Output Data. ADATA\_REC and ADATA\_SP are synchronized Record Output, data with reference clock and reference synchronized signal.

|        | BANK1   |       |         |       |         |       |
|--------|---------|-------|---------|-------|---------|-------|
|        | DSP     |       | SSP     |       | I2S     |       |
|        | ADDR    | VALUE | ADDR    | VALUE | ADDR    | VALUE |
| Master | 0x07[0] | 1     | 0x07[0] | 1     | 0x07[0] | 0     |
|        | 0x07[1] | 0     | 0x07[1] | 1     | 0x07[1] | 0     |
|        | 0x07[7] | 1     | 0x07[7] | 1     | 0x07[7] | 1     |
| Slave  | 0x07[0] | 1     | 0x07[0] | 1     | 0x07[0] | 0     |
|        | 0x07[1] | 0     | 0x07[1] | 1     | 0x07[1] | 0     |
|        | 0x07[7] | 0     | 0x07[7] | 0     | 0x07[7] | 0     |

Table 3.2 Record Output Interface configuration

ACLK\_REC is a reference clock of Record Output Data and ASYNC\_REC is reference synchronized signal. ACLK\_REC and ASYNC\_REC signal support slave mode accepted external signals and master mode generating clock and synchronization signal in itself. And DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively. These figures show timing relation among ASYNC\_REC, ACLK\_REC and ADATA\_REC, and ADATA\_SP is outputted using same interface method of ADATA\_REC. Polarity of ACLK\_REC clock is changed by setting of internal register value (RM\_CLK, 0x07[6], BANK1).

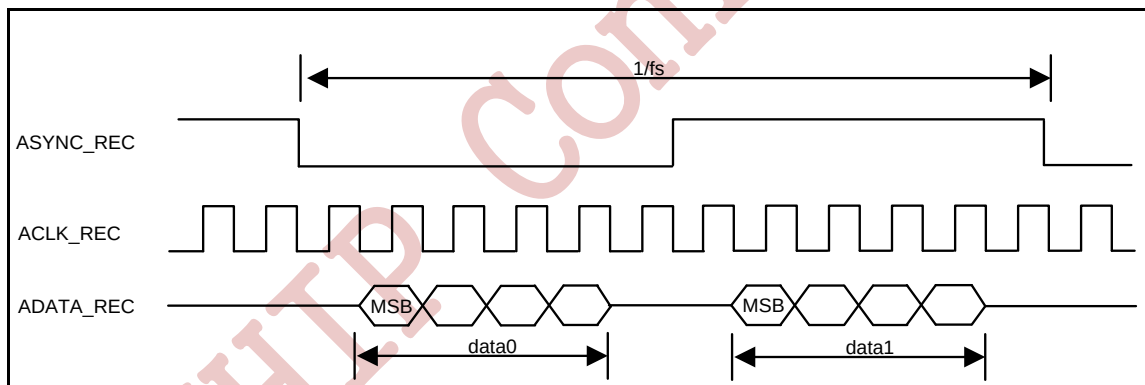


Figure 3.1 Timing of I2S mode

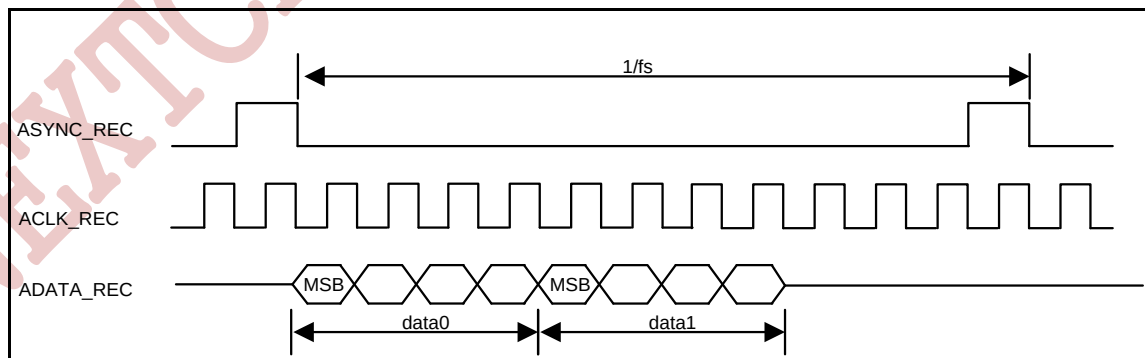


Figure 3.2 Timing of DSP mode

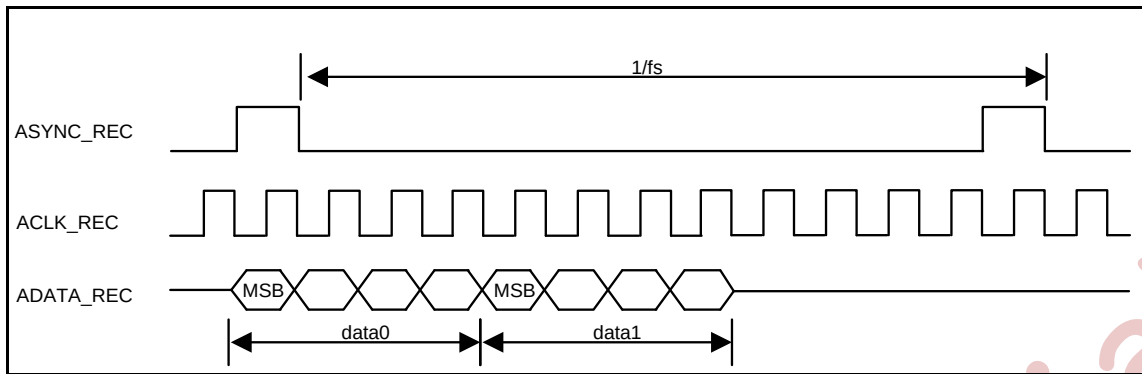


Figure 3.3 Timing of SSP mode

### 3.1.2 2/4/8/16-Channels Data Output(256 fs)

ADATAR\_REC supports up to 8 channel audio using single chip and up to 16 channels audio in cascade mode. In this case, the bit-rate of the audio signal should be 256 fs(RM\_BITRATE, 0x07[5:4], BANK1). The number of output channel is configured by internal register value (R\_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R\_SEQ, 0x09 ~ 0x12, / MIC\_SEQ, 0x3C ~ 0x3D, BANK1).

Therefore, the order of audio output can be changed.

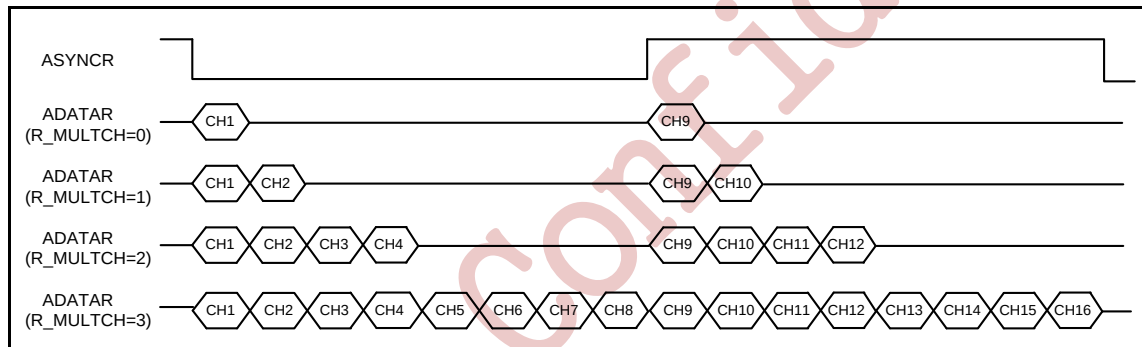


Figure 3.4 audio 2/4/8/16 channels data output <I2S mode, 256fs>

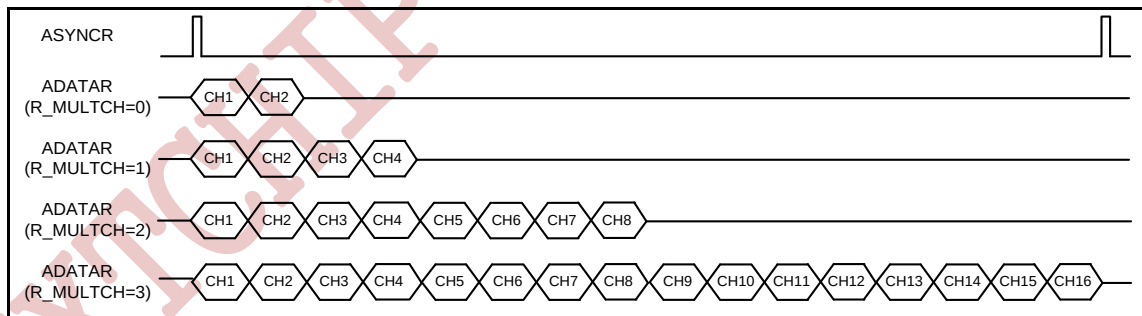


Figure 3.5 audio 2/4/8/16channels data output <DSP/SSP mode, 256fs>

### 3.1.3 2/4/8/16-Channels Audio Data Output with 4-Channels Mic Data(320 fs)

ADATA\_REC supports up to 5 channels(4-Ch audio/1-Ch mic) using single chip and up to 18 channels(16-Ch audio/2-Ch mic) in cascade mode. In this case, the bit-rate of the audio signal should be 320 fs(RM\_BITRATE, 0x07[5:4], BANK1). The number of output channel is configured by internal register value (R\_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R\_SEQ, 0x09 ~ 0x12, / MIC\_SEQ, 0x3C ~ 0x3D, BANK1). Therefore, the order of audio output can be changed.

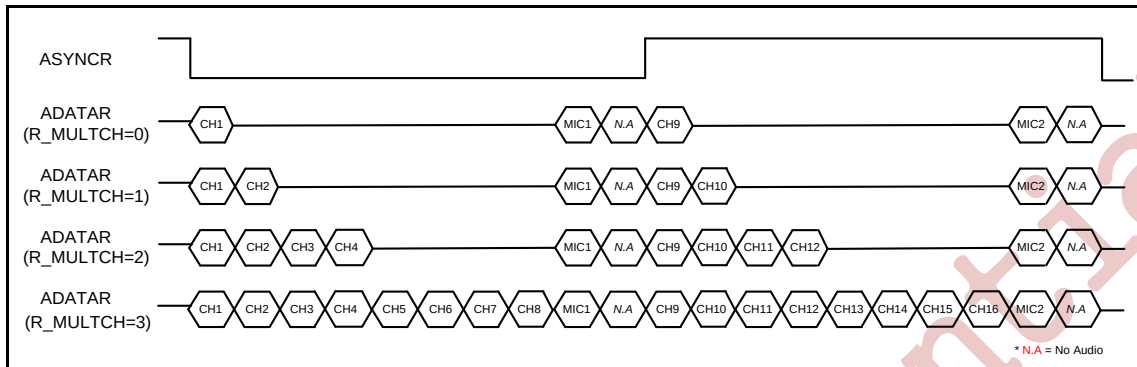


Figure 3.6 audio 2/4/6/8/16 channels data output(with 2 channels mic) <I2S mode, 320fs>

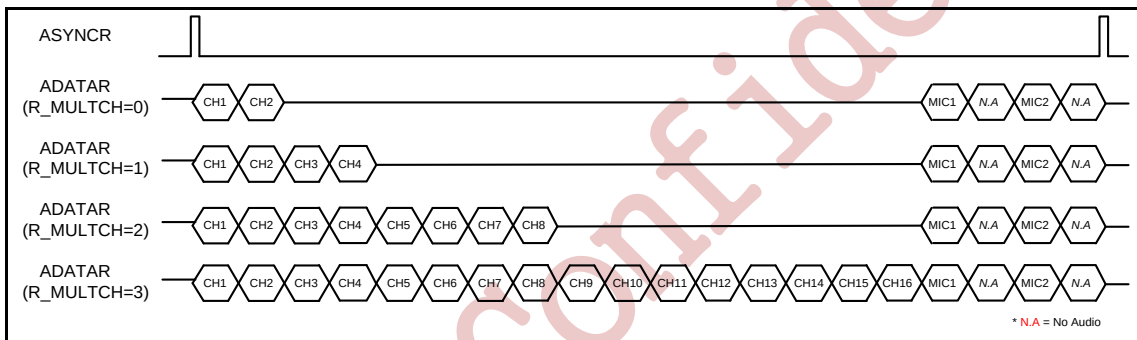


Figure 3.7 audio 2/4/8/16 channels data output(with 2 channels mic) <DSP/SSP mode, 320fs>

### 3.1.4 ADATA\_SP Output

ADATA\_SP supports 3 kinds of output method. Firstly, the output data of ADATA\_SP pin is the exactly same as those of ADATA\_REC except output data sequence. The order of output data is opposite. If the output data order of ADATA\_REC is "CH1, CH2, CH9, CH10", the output data order of ADATA\_SP is "CH16, CH15, CH8, CH7". That is to say, two output pin - ADATA\_SP and ADATA\_REC are complement relationship.

Secondly, one of input signals is selected as output signal of ADATA\_SP. The selectable input signal ranges from analog input signal to ADATA\_PB signal. Lastly, mixed data of input signal is selected as the output signal of ADATA\_SP. The mixing gain of each channel's input signal is determined by internal register setting value (MIX\_RATIO, 0x16 ~ 0x21[7:0], BANK1).

The output configuration of ADATA\_SP is determined by internal register setting. First and second configuration are determined by (R\_ADATSP, 0x08[2], BANK1), and second and third configuration are determined by (L\_CH\_OUTSEL, 0x24[4:0], BANK1) and (R\_CH\_OUTSEL, 0x25[4:0], BANK1). In this case, L\_CH\_OUTSEL and R\_CH\_OUTSEL select one of input channels or mixed data.

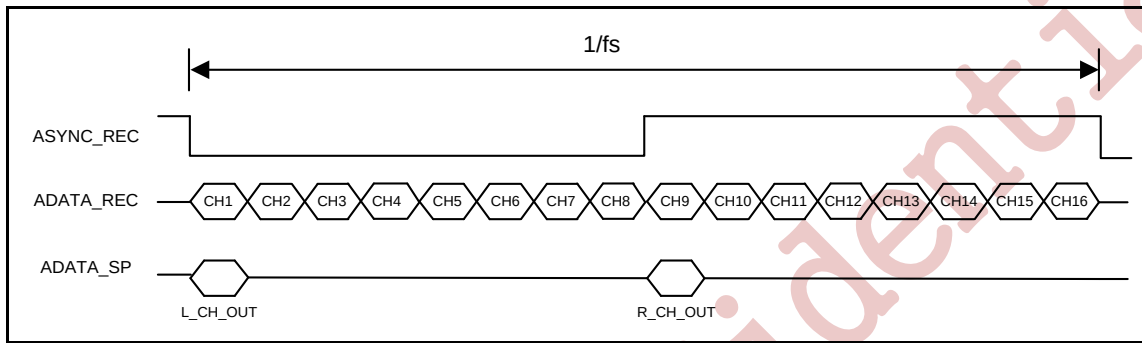


Figure 3.8 ADATA\_SP Output <I2S mode>

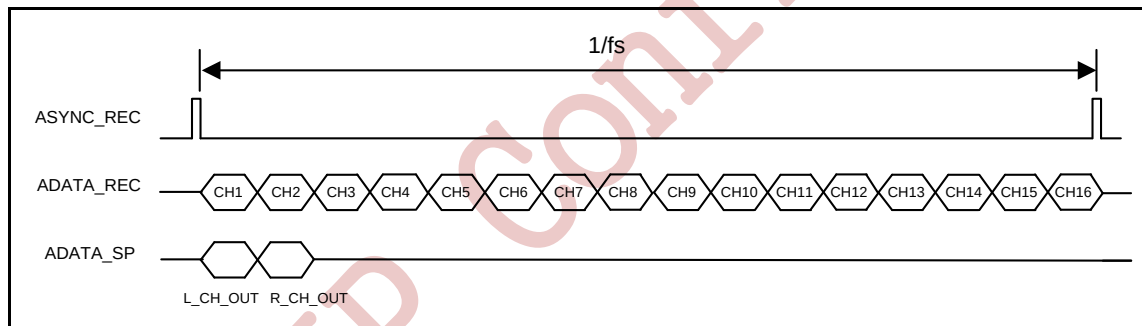


Figure 3.9 ADATA\_SP Output <DSP/SSP mode>

## 3.2 Playback Output

Playback is to output stored audio data to external device through DAC after internal processing.

**NVP6134C** gives and takes a clock and synchronization signal through **ACLK\_PB** and **ASYNC\_PB** pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting (**PB\_SER**, 0x14[4:0], **BANK1**). In case of single channel, **PB\_SEL** should be set to "00000".

**ACLK\_PB** and **ASYNC\_PB** supports Master mode and Slave mode. In master mode, **ACLK\_PB** and **ASYNC\_PB** are outputted by **NVP6134C**, and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register (**PB\_MASTER**, 0x13[7], **BANK1**).

**ADATA\_PB** accepts an audio data synchronized with **ACLK\_PB** and **ASYNC\_PB**. **ACLK\_PB** and **ASYNC\_PB** accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value (**PB\_SYNC**, 0x13[0], **BANK1**). When DSP mode is selected, DSP/SSP mode is set by (**PB\_SSP**, 0x13[1], **BANK1**). The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. **PB\_CLK** can be inverted for all modes using setting of register(**PB\_CLK**, 0x13[6], **BANK1**).

## 3.3 Audio Detection

**NVP6134C** has an audio mute detection block for individual 5 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the **ADET\_MODE**(0x29[3], **BANK1**) and **ADET\_FILT** (0x29[2:0], **BANK1**) register. According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

## 3.4 Cascade Operation

**NVP6134C** supports cascade mode. Maximum 4-**NVP6134C** chips can be connected together for cascade mode and can be processed 18 channel audio encoding data(16-Ch Audio/2-Ch mic). Cascade is enabled by setting register(**CHIP\_STAGE**, 0x06[1:0], **BANK1**). Figure 3.10 shows how to connect **NVP6134C** for the cascade mode. In this case, analog audio **AOUT1** is assigned to **AIN1-16** and **MICIN1-2**. 1 channel audio or all channel mixed audio signal is selected as output signal set by **MIX\_OUTSEL**(0x23[4:0], **BANK1**).

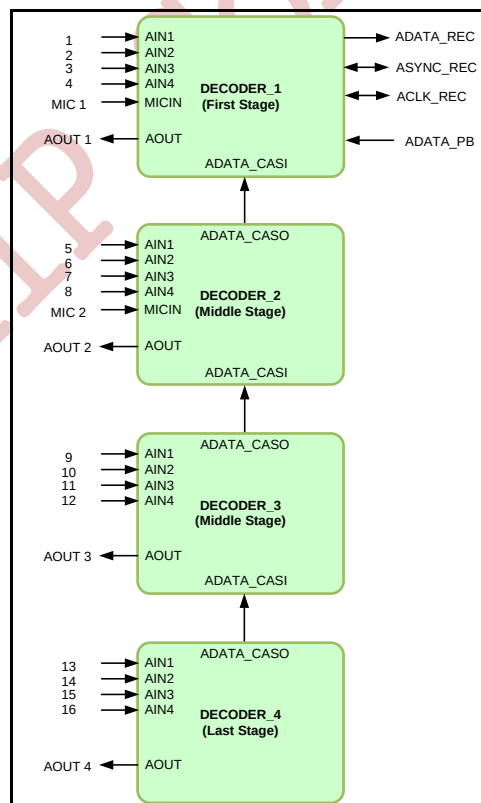


Figure 3.10 Consist of Cascade System using 4-NVP6134C



# Chapter 4

## COAXIAL PROTOCOL

**NVP6134C** includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. **NVP6134C** supports Protocol for CVBS/COMET(PELCO) & AHD(A-CP). It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up The Coax" or "UTC")

### 4.1 PELCO PROTOCOL

There are two types of Coaxitron command structures. One type, Standard Coaxitron, is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 4.1. No pulses are sent when the system is in an idle state

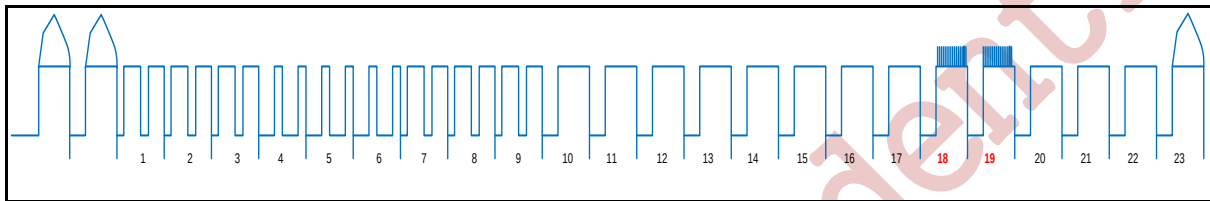


Figure 4.1 Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.2. and Figure 4.3.

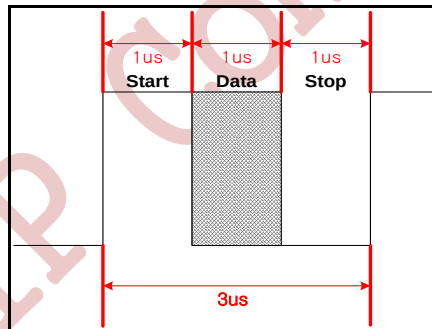


Figure 4.2 Description of One Coaxitron Bit

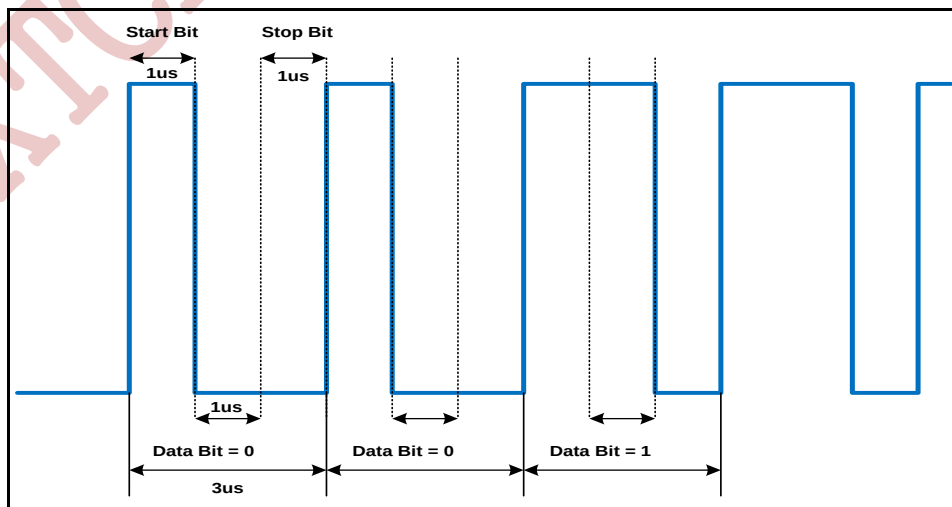


Figure 4.3 Coaxitron Bit Timing

NVP6134C is able to control coaxitron timing format on the video signal.

Start Active line of Coaxitron (BL\_TXST, 0x03~04[3:0], 0x83~84[3:0], BANK3~4) is 18<sup>th</sup> line on VBI. Pulse width of Coaxitron (BAUD, 0x00/0x80, BANK3~4) is fixed 1us. The size of Coaxial Data (PELCO\_TXDAT, 0x20~23, 0xA0~A3, BANK3~4) is 4 bytes. Refer to Figure 4.4.

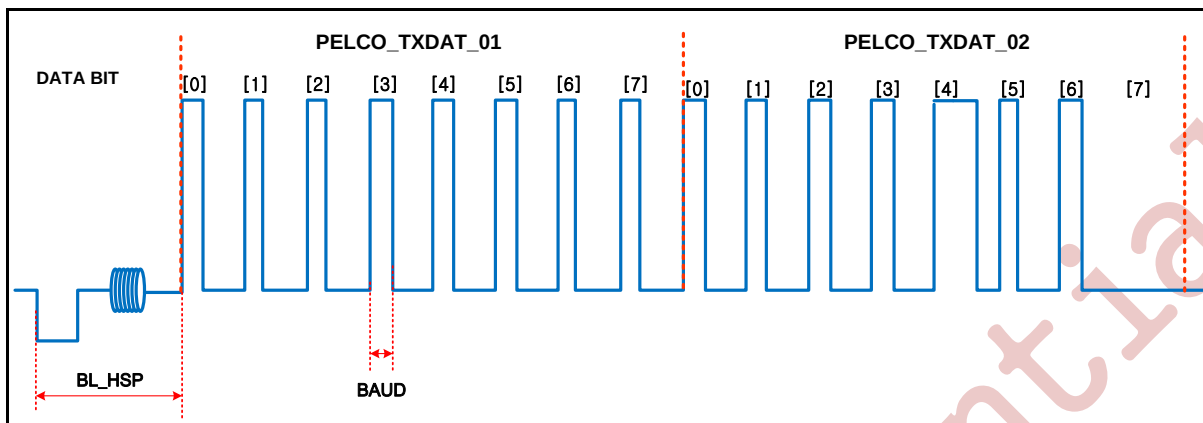


Figure 4.4 Data Structure of Coaxitron Origins (VBI 18th)

## 4.2 A-CP(AHD-Coaxial protocol)

It is an acronym of AHD Coaxial Protocol. This term signifies the interactive communication protocol between Image Signal Processor. As a major feature, A-CP Data located in the 17~20<sup>th</sup> line. Also Data is 8bit each line.

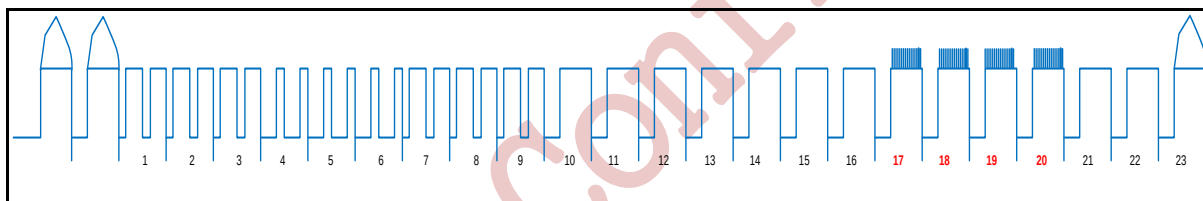


Figure 4.5 A-CP Active line

A-CP is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 1.8us pulse represents a one(1) and a 0.6us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.6. and Figure 4.7.

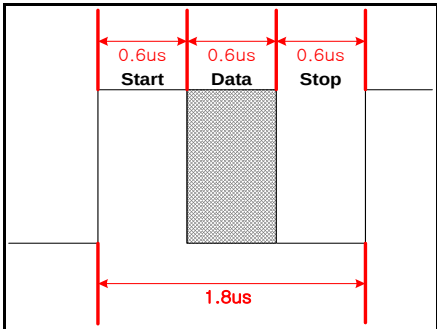


Figure 4.6 Description of A-CP One Data Bit

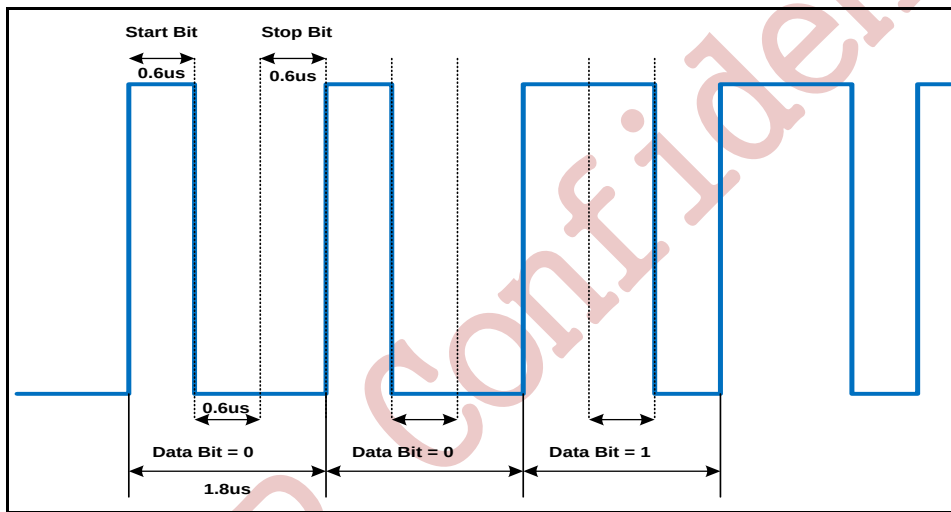


Figure 4.7 Data A-CP Bit Timing

Start Active line of Coaxitron (BL\_TXST, 0x0D~0E[3:0],0x8D~8E[3:0], BANK3~4) is 17<sup>th</sup> line on VBI. Pulse width of Coaxitron (BAUD, 0x00/0x80, BANK3~4) is fixed 0.6us. The size of Coaxial Data (TX\_DATA, 0x10~17, 0x90~0x97, BANK3~4) is 4 bytes. Refer to Figure 4.8.

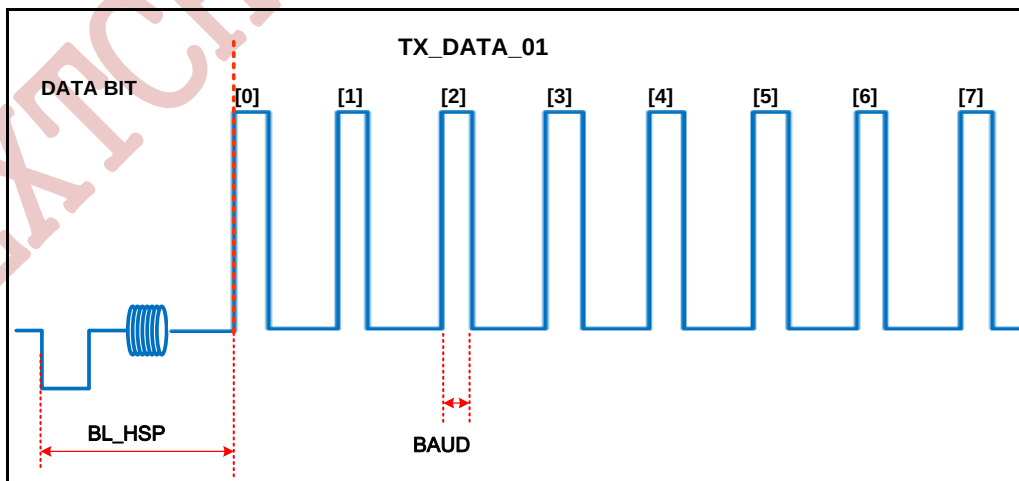


Figure 4.8 Data Structure of Coaxitron Origins (VBI 17th)

# Chapter 5

## I2C INTERFACE

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **NVP6134C** provides special device ID as slave addresses (SA0, SA1). So any combination of 7 bit can be defined as slave address of **NVP6134C**. The Figure 5.1 shows read/write protocol of I2C interface. The 1st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers data to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 5.2.

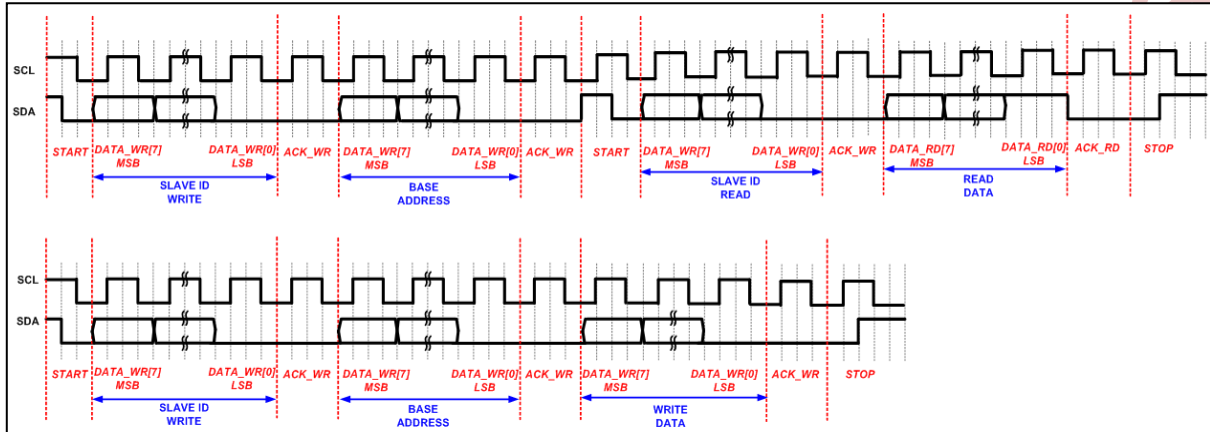


Figure 5.1 I2C Timing Diagram

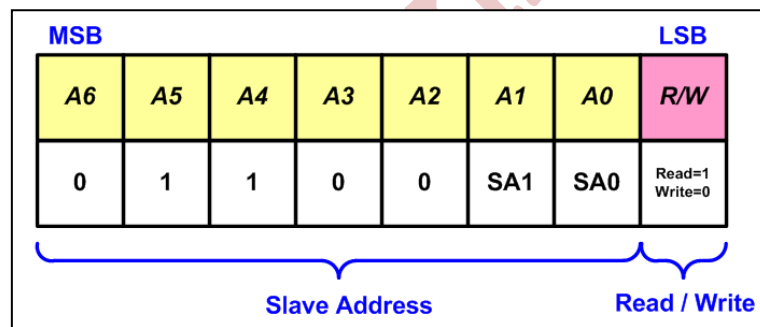


Figure 5.2 I2C Slave Address Configuration

# Chapter 6

## REGISTER DESCRIPTION

### 6.1 REGISTER ADDRESS

#### 6.1.1 BANK0 Register(0x00~0x1F) : VIDEO

| ADDRESS               |      | [7]           | [6]        | [5] | [4]            | [3]           | [2] | [1] | [0]     | Def. | 30P  | 25P  |
|-----------------------|------|---------------|------------|-----|----------------|---------------|-----|-----|---------|------|------|------|
| B<br>A<br>N<br>K<br>0 | 0x00 |               |            |     | -RESERVED-     |               |     |     | PD_VCH1 | 0x01 | 0x00 | 0x00 |
|                       | 0x01 |               |            |     | -RESERVED-     |               |     |     | PD_VCH2 | 0x01 | 0x00 | 0x00 |
|                       | 0x02 |               |            |     | -RESERVED-     |               |     |     | PD_VCH3 | 0x01 | 0x00 | 0x00 |
|                       | 0x03 |               |            |     | -RESERVED-     |               |     |     | PD_VCH4 | 0x01 | 0x00 | 0x00 |
|                       | 0x08 | AUTO_1        | BSF_MODE_1 |     | VIDEO_FORMAT_1 |               |     |     |         | 0x00 | 0x00 | 0x00 |
|                       | 0x09 | AUTO_2        | BSF_MODE_2 |     | VIDEO_FORMAT_2 |               |     |     |         | 0x00 | 0x00 | 0x00 |
|                       | 0x0A | AUTO_3        | BSF_MODE_3 |     | VIDEO_FORMAT_3 |               |     |     |         | 0x00 | 0x00 | 0x00 |
|                       | 0x0B | AUTO_4        | BSF_MODE_4 |     | VIDEO_FORMAT_4 |               |     |     |         | 0x00 | 0x00 | 0x00 |
|                       | 0x0C | BRIGHTNESS_1  |            |     |                |               |     |     |         | 0x08 | 0xED | 0xED |
|                       | 0x0D | BRIGHTNESS_2  |            |     |                |               |     |     |         | 0x08 | 0xED | 0xED |
|                       | 0x0E | BRIGHTNESS_3  |            |     |                |               |     |     |         | 0x08 | 0xED | 0xED |
|                       | 0x0F | BRIGHTNESS_4  |            |     |                |               |     |     |         | 0x08 | 0xED | 0xED |
|                       | 0x10 | CONTRAST_1    |            |     |                |               |     |     |         | 0x88 | 0x88 | 0x88 |
|                       | 0x11 | CONTRAST_2    |            |     |                |               |     |     |         | 0x88 | 0x88 | 0x88 |
|                       | 0x12 | CONTRAST_3    |            |     |                |               |     |     |         | 0x88 | 0x88 | 0x88 |
|                       | 0x13 | CONTRAST_4    |            |     |                |               |     |     |         | 0x88 | 0x88 | 0x88 |
|                       | 0x14 | H_SHARPNESS_1 |            |     |                | V_SHARPNESS_1 |     |     |         | 0x90 | 0x90 | 0x90 |
|                       | 0x15 | H_SHARPNESS_2 |            |     |                | V_SHARPNESS_2 |     |     |         | 0x90 | 0x90 | 0x90 |
|                       | 0x16 | H_SHARPNESS_3 |            |     |                | V_SHARPNESS_3 |     |     |         | 0x90 | 0x90 | 0x90 |
|                       | 0x17 | H_SHARPNESS_4 |            |     |                | V_SHARPNESS_4 |     |     |         | 0x90 | 0x90 | 0x90 |
|                       | 0x18 | Y_PEAK_MODE_1 |            |     |                | Y_FIR_MODE_1  |     |     |         | 0x00 | 0x20 | 0x20 |
|                       | 0x19 | Y_PEAK_MODE_2 |            |     |                | Y_FIR_MODE_2  |     |     |         | 0x00 | 0x20 | 0x20 |
|                       | 0x1A | Y_PEAK_MODE_3 |            |     |                | Y_FIR_MODE_3  |     |     |         | 0x00 | 0x20 | 0x20 |
|                       | 0x1B | Y_PEAK_MODE_4 |            |     |                | Y_FIR_MODE_4  |     |     |         | 0x00 | 0x20 | 0x20 |

### 6.1.2 BANK0 Register(0x20~0x3F) : VIDEO

| ADDRESS |      | [7]          | [6]          | [5]        | [4]        | [3]        | [2] | [1]  | [0]  | Def. | 30P  | 25P  |
|---------|------|--------------|--------------|------------|------------|------------|-----|------|------|------|------|------|
| BANK0   | 0x21 | PAL_CM_OFF_1 | IF_FIR_SEL_1 |            |            | CLPF_SEL_1 |     |      |      | 0x92 | 0x92 | 0x92 |
|         | 0x22 |              |              |            | COLOROFF_1 | C_KILL_1   |     |      |      | 0x0A | 0x0B | 0x0B |
|         | 0x25 | PAL_CM_OFF_2 | IF_FIR_SEL_2 |            |            | CLPF_SEL_2 |     |      |      | 0x92 | 0x92 | 0x92 |
|         | 0x26 |              |              |            | COLOROFF_2 | C_KILL_2   |     |      |      | 0x0A | 0x0B | 0x0B |
|         | 0x29 | PAL_CM_OFF_3 | IF_FIR_SEL_3 |            |            | CLPF_SEL_3 |     |      |      | 0x92 | 0x92 | 0x92 |
|         | 0x2A |              |              |            | COLOROFF_3 | C_KILL_3   |     |      |      | 0x0A | 0x0B | 0x0B |
|         | 0x2D | PAL_CM_OFF_4 | IF_FIR_SEL_4 |            |            | CLPF_SEL_4 |     |      |      | 0x92 | 0x92 | 0x92 |
|         | 0x2E |              |              |            | COLOROFF_4 | C_KILL_4   |     |      |      | 0x0A | 0x0B | 0x0B |
|         | 0x30 | -RESERVED-   |              |            | Y_DELAY_1  |            |     |      | 0x12 | 0x10 | 0x10 |      |
|         | 0x31 | -RESERVED-   |              |            | Y_DELAY_2  |            |     |      | 0x12 | 0x10 | 0x10 |      |
|         | 0x32 | -RESERVED-   |              |            | Y_DELAY_3  |            |     |      | 0x12 | 0x10 | 0x10 |      |
|         | 0x33 | -RESERVED-   |              |            | Y_DELAY_4  |            |     |      | 0x12 | 0x10 | 0x10 |      |
|         | 0x34 | -RESERVED-   | PED_ON_1     | -RESERVED- |            |            |     | 0x02 | 0x04 | 0x02 |      |      |
|         | 0x35 | -RESERVED-   | PED_ON_2     | -RESERVED- |            |            |     | 0x02 | 0x04 | 0x02 |      |      |
|         | 0x36 | -RESERVED-   | PED_ON_3     | -RESERVED- |            |            |     | 0x02 | 0x04 | 0x02 |      |      |
|         | 0x37 | -RESERVED-   | PED_ON_4     | -RESERVED- |            |            |     | 0x02 | 0x04 | 0x02 |      |      |
|         | 0x38 | CTI_GAIN_1   |              |            |            |            |     |      |      | 0x0A | 0x0A | 0x0A |
|         | 0x39 | CTI_GAIN_2   |              |            |            |            |     |      |      | 0x0A | 0x0A | 0x0A |
|         | 0x3A | CTI_GAIN_3   |              |            |            |            |     |      |      | 0x0A | 0x0A | 0x0A |
|         | 0x3B | CTI_GAIN_4   |              |            |            |            |     |      |      | 0x0A | 0x0A | 0x0A |
|         | 0x3C | SATURATION_1 |              |            |            |            |     |      |      | 0x90 | 0x84 | 0x84 |
|         | 0x3D | SATURATION_2 |              |            |            |            |     |      |      | 0x90 | 0x84 | 0x84 |
|         | 0x3E | SATURATION_3 |              |            |            |            |     |      |      | 0x90 | 0x84 | 0x84 |
|         | 0x3F | SATURATION_4 |              |            |            |            |     |      |      | 0x90 | 0x84 | 0x84 |

### 6.1.3 BANK0 Register(0x40~0x5F) : VIDEO

| ADDRESS |      | [7]        | [6]       | [5]       | [4]       | [3]             | [2]          | [1] | [0] | Def. | 30P  | 25P  |
|---------|------|------------|-----------|-----------|-----------|-----------------|--------------|-----|-----|------|------|------|
| BANK0   | 0x40 | HUE_1      |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x41 | HUE_2      |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x42 | HUE_3      |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x43 | HUE_4      |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x44 | U_GAIN_1   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x45 | U_GAIN_2   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x46 | U_GAIN_3   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x47 | U_GAIN_4   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x48 | V_GAIN_1   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x49 | V_GAIN_2   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4A | V_GAIN_3   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4B | V_GAIN_4   |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4C | U_OFFSET_1 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4D | U_OFFSET_2 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4E | U_OFFSET_3 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x4F | U_OFFSET_4 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x50 | V_OFFSET_1 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x51 | V_OFFSET_2 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x52 | V_OFFSET_3 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x53 | V_OFFSET_4 |           |           |           |                 |              |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x54 | FLD_INV_4  | FLD_INV_3 | FLD_INV_2 | FLD_INV_1 | NOVID_INF_IN_14 | CHID_TYPE_14 |     |     | 0x01 | 0xF1 | 0x01 |
|         | 0x55 | CHID_VIN2  |           |           |           | CHID_VIN1       |              |     |     | 0x10 | 0x10 | 0x10 |
|         | 0x56 | CHID_VIN4  |           |           |           | CHID_VIN3       |              |     |     | 0x10 | 0x10 | 0x10 |
|         | 0x58 | H_DELAY_1  |           |           |           |                 |              |     |     | 0x80 | 0x8B | 0x80 |
|         | 0x59 | H_DELAY_2  |           |           |           |                 |              |     |     | 0x80 | 0x8B | 0x80 |
|         | 0x5A | H_DELAY_3  |           |           |           |                 |              |     |     | 0x80 | 0x8B | 0x80 |
|         | 0x5B | H_DELAY_4  |           |           |           |                 |              |     |     | 0x80 | 0x8B | 0x80 |
|         | 0x5C | V_DELAY_1  |           |           |           |                 |              |     |     | 0x00 | 0x9E | 0x9E |
|         | 0x5D | V_DELAY_2  |           |           |           |                 |              |     |     | 0x00 | 0x9E | 0x9E |
|         | 0x5E | V_DELAY_3  |           |           |           |                 |              |     |     | 0x00 | 0x9E | 0x9E |
|         | 0x5F | V_DELAY_4  |           |           |           |                 |              |     |     | 0x00 | 0x9E | 0x9E |

# 6.1.4 BANK0 Register(0x60~0x7F) : VIDEO

| ADDRESS | [7]  | [6]             | [5] | [4] | [3]             | [2] | [1] | [0] | Def. | 30P  | 25P  |
|---------|------|-----------------|-----|-----|-----------------|-----|-----|-----|------|------|------|
| BANK0   | 0x60 | HBLK_END_1      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x61 | HBLK_END_2      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x62 | HBLK_END_3      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x63 | HBLK_END_4      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x64 | VBLK_END_1      |     |     |                 |     |     |     | 0x00 | 0xC0 | 0xC0 |
|         | 0x65 | VBLK_END_2      |     |     |                 |     |     |     | 0x00 | 0xC0 | 0xC0 |
|         | 0x66 | VBLK_END_3      |     |     |                 |     |     |     | 0x00 | 0xC0 | 0xC0 |
|         | 0x67 | VBLK_END_4      |     |     |                 |     |     |     | 0x00 | 0xC0 | 0xC0 |
|         | 0x68 | H_CROP_S_1      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x69 | H_CROP_S_2      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6A | H_CROP_S_3      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6B | H_CROP_S_4      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6C | H_CROP_E_1      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6D | H_CROP_E_2      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6E | H_CROP_E_3      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x6F | H_CROP_E_4      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x70 | V_CROP_S_1      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x71 | V_CROP_S_2      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x72 | V_CROP_S_3      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x73 | V_CROP_S_4      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x74 | V_CROP_E_1      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x75 | V_CROP_E_2      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x76 | V_CROP_E_3      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x77 | V_CROP_E_4      |     |     |                 |     |     |     | 0x00 | 0x00 | 0x00 |
|         | 0x78 | BGDCOL_2        |     |     | BGDCOL_1        |     |     |     | 0x88 | 0x88 | 0x88 |
|         | 0x79 | BGDCOL_4        |     |     | BGDCOL_3        |     |     |     | 0x88 | 0x88 | 0x88 |
|         | 0x7A | DATA_OUT_MODE_2 |     |     | DATA_OUT_MODE_1 |     |     |     | 0x11 | 0x11 | 0x11 |
|         | 0x7B | DATA_OUT_MODE_4 |     |     | DATA_OUT_MODE_3 |     |     |     | 0x11 | 0x11 | 0x11 |



### 6.1.5 BANK0 Register(0x80~0xA3) : VIDEO\_ENABLE & Delay

| ADDRESS |      | [7]         | [6] | [5] | [4] | [3]          | [2] | [1] | [0]        | Def. | 30P  | 25P  |
|---------|------|-------------|-----|-----|-----|--------------|-----|-----|------------|------|------|------|
| BANK0   | 0x80 |             |     |     |     | EACH_REG_SET |     |     |            | 0x00 | 0x0F | 0x0F |
|         | 0x81 | SD_MD_1     |     |     |     | AHD_MD_1     |     |     |            | 0x03 | 0x02 | 0x03 |
|         | 0x82 | SD_MD_2     |     |     |     | AHD_MD_2     |     |     |            | 0x03 | 0x02 | 0x03 |
|         | 0x83 | SD_MD_3     |     |     |     | AHD_MD_3     |     |     |            | 0x03 | 0x02 | 0x03 |
|         | 0x84 | SD_MD_4     |     |     |     | AHD_MD_4     |     |     |            | 0x03 | 0x02 | 0x03 |
|         | 0x8E | H_DLY_MSB_1 |     |     |     | -RESERVED-   |     |     |            | 0x09 | 0x00 | 0x00 |
|         | 0x8F | H_DLY_MSB_2 |     |     |     | -RESERVED-   |     |     |            | 0x09 | 0x00 | 0x00 |
|         | 0x90 | H_DLY_MSB_3 |     |     |     | -RESERVED-   |     |     |            | 0x09 | 0x00 | 0x00 |
|         | 0x91 | H_DLY_MSB_4 |     |     |     | -RESERVED-   |     |     |            | 0x09 | 0x00 | 0x00 |
|         | 0x93 | -RESERVED-  |     |     |     |              |     |     | HZOOM_ON_1 | 0x00 | 0x00 | 0x00 |
|         | 0x94 | -RESERVED-  |     |     |     |              |     |     | HZOOM_ON_2 | 0x00 | 0x00 | 0x00 |
|         | 0x95 | -RESERVED-  |     |     |     |              |     |     | HZOOM_ON_3 | 0x00 | 0x00 | 0x00 |
|         | 0x96 | -RESERVED-  |     |     |     |              |     |     | HZOOM_ON_4 | 0x00 | 0x00 | 0x00 |
|         | 0x98 | -RESERVED-  |     |     |     | H_ZOOM.DTO_1 |     |     |            | 0x07 | 0x00 | 0x00 |
|         | 0x99 | -RESERVED-  |     |     |     | H_ZOOM.DTO_2 |     |     |            | 0x07 | 0x00 | 0x00 |
|         | 0x9A | -RESERVED-  |     |     |     | H_ZOOM.DTO_3 |     |     |            | 0x07 | 0x00 | 0x00 |
|         | 0x9B | -RESERVED-  |     |     |     | H_ZOOM.DTO_4 |     |     |            | 0x07 | 0x00 | 0x00 |
|         | 0xA0 | DF_CDELAY_1 |     |     |     | DF_YDELAY_1  |     |     |            | 0x00 | 0x00 | 0x00 |
|         | 0xA1 | DF_CDELAY_2 |     |     |     | DF_YDELAY_2  |     |     |            | 0x00 | 0x00 | 0x00 |
|         | 0xA2 | DF_CDELAY_3 |     |     |     | DF_YDELAY_3  |     |     |            | 0x00 | 0x00 | 0x00 |
|         | 0xA3 | DF_CDELAY_4 |     |     |     | DF_YDELAY_4  |     |     |            | 0x00 | 0x00 | 0x00 |

# 6.1.6 BANK0 Register(0xA8~0xF5) : STATUS

| ADDRESS | [7]                      | [6]      | [5]      | [4]        | [3]             | [2]             | [1]              | [0]             | Def. | 30P  | 25P  |
|---------|--------------------------|----------|----------|------------|-----------------|-----------------|------------------|-----------------|------|------|------|
| 0xA8    |                          |          |          |            | NOVID_04        | NOVID_03        | NOVID_02         | NOVID_01        | R    | R    | R    |
| 0xA9    |                          |          |          |            | MOTION_04       | MOTION_03       | MOTION_02        | MOTION_01       | R    | R    | R    |
| 0xAC    | MUTE_08                  | MUTE_07  | MUTE_06  | MUTE_05    | MUTE_04         | MUTE_03         | MUTE_02          | MUTE_01         | R    | R    | R    |
| 0xAD    | MUTE_16                  | MUTE_15  | MUTE_14  | MUTE_13    | MUTE_12         | MUTE_11         | MUTE_10          | MUTE_09         | R    | R    | R    |
| 0xAE    |                          |          |          |            |                 |                 | MUTEMIC_02       | MUTEMIC_01      | R    | R    | R    |
| 0xAF    |                          |          |          |            | COAX_RX_DONE_4  | COAX_RX_DONE_3  | COAX_RX_DONE_2   | COAX_RX_DONE_1  | R    | R    | R    |
| 0xB0    |                          |          |          |            | NOVID_04B       | NOVID_03B       | NOVID_02B        | NOVID_01B       | R    | R    | R    |
| 0xB1    |                          |          |          |            | MOTION_04B      | MOTION_03B      | MOTION_02B       | MOTION_01B      | R    | R    | R    |
| 0xB4    | MUTE_08B                 | MUTE_07B | MUTE_06B | MUTE_05B   | MUTE_04B        | MUTE_03B        | MUTE_02B         | MUTE_01B        | R    | R    | R    |
| 0xB5    | MUTE_16B                 | MUTE_15B | MUTE_14B | MUTE_13B   | MUTE_12B        | MUTE_11B        | MUTE_10B         | MUTE_09B        | R    | R    | R    |
| 0xB6    |                          |          |          |            |                 |                 | MUTEMIC_02B      | MUTEMIC_01B     | R    | R    | R    |
| 0xB7    |                          |          |          |            | COAX_RX_DONE_4B | COAX_RX_DONE_3B | COAX_RX_DONE_2B  | COAX_RX_DONE_1B | R    | R    | R    |
| 0xB8    | RD_STATE_CLR             |          |          | STATE_HOLD |                 |                 |                  |                 | 0x90 | 0x90 | 0x90 |
| 0xB9    |                          |          |          | IRQ_MSB    | IRQ_INV         | IRQ_SEL         |                  |                 | 0x00 | 0x00 | 0x00 |
| 0xE0    |                          |          |          |            | AGC_LOCK_04     | AGC_LOCK_03     | AGC_LOCK_02      | AGC_LOCK_01     | R    | R    | R    |
| 0xE1    |                          |          |          |            | CMP_LOCK_04     | CMP_LOCK_03     | CMP_LOCK_02      | CMP_LOCK_01     | R    | R    | R    |
| 0xE2    |                          |          |          |            | H_LOCK_04       | H_LOCK_03       | H_LOCK_02        | H_LOCK_01       | R    | R    | R    |
| 0xE7    |                          |          |          |            | BW_04           | BW_03           | BW_02            | BW_01           | R    | R    | R    |
| 0xE8    | -RESERVED-               |          |          |            | FSC_CHG_DONE_01 | CKILL_01        | FSC_LOCK_DONE_01 | NOVIDEO_01      | R    | R    | R    |
| 0xE9    | -RESERVED-               |          |          |            | FSC_CHG_DONE_02 | CKILL_02        | FSC_LOCK_DONE_02 | NOVIDEO_02      | R    | R    | R    |
| 0xEA    | -RESERVED-               |          |          |            | FSC_CHG_DONE_03 | CKILL_03        | FSC_LOCK_DONE_03 | NOVIDEO_03      | R    | R    | R    |
| 0xEB    | -RESERVED-               |          |          |            | FSC_CHG_DONE_04 | CKILL_04        | FSC_LOCK_DONE_04 | NOVIDEO_04      | R    | R    | R    |
| 0xF4    | DEV_ID (NVP6134C = 0x90) |          |          |            |                 |                 |                  |                 | R    | R    | R    |
| 0xF5    | REV_ID (0x01)            |          |          |            |                 |                 |                  |                 | R    | R    | R    |

# 6.1.7 BANK1 Register(0x00~0x1E) : AUDIO

| ADDRESS |      | [7]           | [6]         | [5]         | [4]         | [3]           | [2]         | [1]         | [0]         | Def. | 30P  | 25P  |      |
|---------|------|---------------|-------------|-------------|-------------|---------------|-------------|-------------|-------------|------|------|------|------|
| BANK 1  | 0x00 | PD_AU_AFE     | PD_AU_DAC   |             |             | RM_PB_PIN     | PB_RM_PIN   | FILTER_ON   | EN_32K_MODE | 0x02 | 0x02 | 0x02 |      |
|         | 0x01 | AIGAIN_01     |             |             |             |               |             |             |             | 0x00 | 0x08 | 0x08 |      |
|         | 0x02 | AIGAIN_02     |             |             |             |               |             |             |             | 0x00 | 0x08 | 0x08 |      |
|         | 0x03 | AIGAIN_03     |             |             |             |               |             |             |             | 0x00 | 0x08 | 0x08 |      |
|         | 0x04 | AIGAIN_04     |             |             |             |               |             |             |             | 0x00 | 0x08 | 0x08 |      |
|         | 0x05 | MIGAIN_01     |             |             |             |               |             |             |             | 0x00 | 0x08 | 0x08 |      |
|         | 0x06 | CAS_PB        | TRANS_MODE  | CAS_4CH     | CAS_PIN     | CASCADE_MODE  | -RESERVED-  | CHIP_STAGE  |             | 0x1B | 0x3B | 0x3B |      |
|         | 0x07 | RM_MASTER     | RM_CLK      | RM_BITRATE  |             | RM_SAMRATE    | RM_BITWID   | RM_SSP      | RM_SYNC     | 0xC8 | 0xC8 | 0xC8 |      |
|         | 0x08 | RM_BIT_SWAP   | RM_LAW_SEL  | RM_FORMAT   |             | -RESERVED-    | R_ADATSP    | R_MULTCH    |             | 0x03 | 0x03 | 0x03 |      |
|         | 0x09 | R_SEQ_08[4]   | R_SEQ_07[4] | R_SEQ_06[4] | R_SEQ_05[4] | R_SEQ_04[4]   | R_SEQ_03[4] | R_SEQ_02[4] | R_SEQ_01[4] | 0x00 | 0x00 | 0x00 |      |
|         | 0x0A | R_SEQ_02[3:0] |             |             |             | R_SEQ_01[3:0] |             |             |             | 0x10 | 0x10 | 0x10 |      |
|         | 0x0B | R_SEQ_04[3:0] |             |             |             | R_SEQ_03[3:0] |             |             |             | 0x32 | 0x32 | 0x32 |      |
|         | 0x0C | R_SEQ_06[3:0] |             |             |             | R_SEQ_05[3:0] |             |             |             | 0x54 | 0x54 | 0x54 |      |
|         | 0x0D | R_SEQ_08[3:0] |             |             |             | R_SEQ_07[3:0] |             |             |             | 0x76 | 0x76 | 0x76 |      |
|         | 0x0E | R_SEQ_16[4]   | R_SEQ_15[4] | R_SEQ_14[4] | R_SEQ_13[4] | R_SEQ_12[4]   | R_SEQ_11[4] | R_SEQ_10[4] | R_SEQ_09[4] | 0x00 | 0x00 | 0x00 |      |
|         | 0x0F | R_SEQ_10[3:0] |             |             |             | R_SEQ_09[3:0] |             |             |             | 0x98 | 0x98 | 0x98 |      |
|         | 0x10 | R_SEQ_12[3:0] |             |             |             | R_SEQ_11[3:0] |             |             |             | 0xBA | 0xBA | 0xBA |      |
|         | 0x11 | R_SEQ_14[3:0] |             |             |             | R_SEQ_13[3:0] |             |             |             | 0xDC | 0xDC | 0xDC |      |
|         | 0x12 | R_SEQ_16[3:0] |             |             |             | R_SEQ_15[3:0] |             |             |             | 0xFE | 0xFE | 0xFE |      |
|         | 0x13 | PB_MASTER     | PB_CLK      | PB_BITRATE  |             | PB_SAMRATE    | PB_BITWID   | PB_SSP      | PB_SYNC     | 0x08 | 0x08 | 0x08 |      |
|         | 0x14 | PB_BIT_SWAP   |             |             | PB_SEL      |               |             |             |             |      | 0x00 | 0x00 | 0x00 |
|         | 0x15 | PB_FORMAT     |             |             |             | PB_LAW_SEL    | -RESERVED-  |             |             | 0x00 | 0x00 | 0x00 |      |
|         | 0x16 | MIX_RATIO_02  |             |             |             | MIX_RATIO_01  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x17 | MIX_RATIO_04  |             |             |             | MIX_RATIO_03  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x18 | MIX_RATIO_06  |             |             |             | MIX_RATIO_05  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x19 | MIX_RATIO_08  |             |             |             | MIX_RATIO_07  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x1A | MIX_RATIO_10  |             |             |             | MIX_RATIO_09  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x1B | MIX_RATIO_12  |             |             |             | MIX_RATIO_11  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x1C | MIX_RATIO_14  |             |             |             | MIX_RATIO_13  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x1D | MIX_RATIO_16  |             |             |             | MIX_RATIO_15  |             |             |             | 0x88 | 0x88 | 0x88 |      |
|         | 0x1E | MIX_RATIO_M2  |             |             |             | MIX_RATIO_M1  |             |             |             | 0x88 | 0x88 | 0x88 |      |

## 6.1.8 BANK1 Register(0x20~0x44) : AUDIO

| ADDRESS |      | [7]             | [6]         | [5]         | [4]         | [3]          | [2]         | [1]         | [0]         | Def.    | 30P  | 25P  |      |
|---------|------|-----------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|---------|------|------|------|
|         | 0x20 | MIX_RATIO_P2    |             |             |             | MIX_RATIO_P1 |             |             |             | 0x88    | 0x88 | 0x88 |      |
|         | 0x21 | MIX_RATIO_P4    |             |             |             | MIX_RATIO_P3 |             |             |             | 0x88    | 0x88 | 0x88 |      |
|         | 0x22 | AOGAIN          |             |             |             |              |             |             |             | 0x00    | 0x08 | 0x08 |      |
|         | 0x23 |                 |             | MIX_DERATIO | MIX_OUTSEL  |              |             |             |             | 0x19    | 0x19 | 0x19 |      |
|         | 0x24 |                 |             |             | L_CH_OUTSEL |              |             |             |             | 0x18    | 0x19 | 0x19 |      |
|         | 0x25 |                 |             |             | R_CH_OUTSEL |              |             |             |             | 0x16    | 0x19 | 0x19 |      |
| B       | 0x26 | MIX_MUTE_08     | MIX_MUTE_07 | MIX_MUTE_06 | MIX_MUTE_05 | MIX_MUTE_04  | MIX_MUTE_03 | MIX_MUTE_02 | MIX_MUTE_01 | 0x00    | 0x00 | 0x00 |      |
| A       | 0x27 | MIX_MUTE_16     | MIX_MUTE_15 | MIX_MUTE_14 | MIX_MUTE_13 | MIX_MUTE_12  | MIX_MUTE_11 | MIX_MUTE_10 | MIX_MUTE_09 | 0x00    | 0x00 | 0x00 |      |
| N       | 0x28 | -RESERVED-      |             | MIX_MUTE_M2 | MIX_MUTE_M1 | MIX_MUTE_P4  | MIX_MUTE_P3 | MIX_MUTE_P2 | MIX_MUTE_P1 | 0x00    | 0x00 | 0x00 |      |
| K       | 0x29 | AUTO_MUTE       | -RESERVED-  |             |             | ADET_MODE    |             | ADET_FILT   |             | 0x88    | 0x88 | 0x88 |      |
| 1       | 0x2A |                 |             |             |             | ADET_04      |             | ADET_03     | ADET_02     | ADET_01 | 0xFF | 0xFF | 0xFF |
|         | 0x2B |                 | ADET_M1     |             |             |              |             |             |             | 0xC0    | 0x40 | 0x40 |      |
|         | 0x38 | -RESERVED-      |             |             | AUD_SW_RST  |              | -RESERVED-  |             |             | 0x08    | 0x08 | 0x08 |      |
|         | 0x3A |                 |             |             |             | A_DAC_GAIN   |             |             |             | 0xA2    | 0x03 | 0x03 |      |
|         | 0x3B | A_GAIN_SEL(AFE) |             |             |             | -RESERVED-   |             |             |             | 0x30    | 0x30 | 0x30 |      |
|         | 0x3C |                 |             |             | MIC_SEQ_01  |              |             |             |             | 0x00    | 0x10 | 0x10 |      |
|         | 0x3D |                 |             |             | MIC_SEQ_02  |              |             |             |             | 0x00    | 0x11 | 0x11 |      |

### 6.1.9 BANK1 Register(0x80~0x9F) : IP Power Down

| ADDRESS  | [7]  | [6] | [5] | [4]    | [3]     | [2]     | [1]     | [0]     | Def. | 30P  | 25P  |
|----------|------|-----|-----|--------|---------|---------|---------|---------|------|------|------|
| <b>B</b> | 0x97 |     |     |        | CH_RST4 | CH_RST3 | CH_RST2 | CH_RST1 | 0x0F | 0x0F | 0x0F |
| <b>A</b> | 0x98 |     |     |        | PD_DEC4 | PD_DEC3 | PD_DEC2 | PD_DEC1 | 0x00 | 0x00 | 0x00 |
| <b>N</b> | 0x9A |     |     | AU_RST |         |         |         | PD_AUD  | 0x00 | 0x00 | 0x00 |
| <b>K</b> |      |     |     |        |         |         |         |         |      |      |      |
| <b>1</b> |      |     |     |        |         |         |         |         |      |      |      |

### 6.1.10 BANK1 Register(0xB0~0xBF) : MPP

| ADDRESS  | [7]  | [6]          | [5] | [4] | [3]              | [2]      | [1]      | [0]      | Def. | 30P  | 25P  |
|----------|------|--------------|-----|-----|------------------|----------|----------|----------|------|------|------|
| <b>B</b> | 0xB1 |              |     |     | MPP4_DIR         | MPP3_DIR | MPP2_DIR | MPP1_DIR | 0x00 | 0x00 | 0x00 |
| <b>A</b> | 0xB2 |              |     |     | MPP4_CLK         | MPP3_CLK | MPP2_CLK | MPP1_CLK | 0x00 | 0x00 | 0x00 |
| <b>N</b> | 0xB3 |              |     |     | MPP4_INV         | MPP3_INV | MPP2_INV | MPP1_INV | 0x00 | 0x00 | 0x00 |
| <b>K</b> | 0xB4 | MPP_CLK1_SEL |     |     | MPP_CLK1_DLY_SEL |          |          |          | 0x40 | 0x40 | 0x40 |
| <b>1</b> | 0xB5 | MPP_CLK2_SEL |     |     | MPP_CLK2_DLY_SEL |          |          |          | 0x40 | 0x40 | 0x40 |
|          | 0xB6 | MPP_CLK3_SEL |     |     | MPP_CLK3_DLY_SEL |          |          |          | 0x40 | 0x40 | 0x40 |
|          | 0xB7 | MPP_CLK4_SEL |     |     | MPP_CLK4_DLY_SEL |          |          |          | 0x40 | 0x40 | 0x40 |

### 6.1.11 BANK1 Register(0xC2~0xCE) : OUTPUT PORT

| ADDRESS               |      | [7]                | [6]       | [5]       | [4]        | [3]                  | [2]            | [1]            | [0]        | Def. | 30P  | 25P  |
|-----------------------|------|--------------------|-----------|-----------|------------|----------------------|----------------|----------------|------------|------|------|------|
| B<br>A<br>N<br>K<br>1 | 0xC2 | VPORT_1_SEQ2       |           |           |            | VPORT_1_SEQ1         |                |                |            | 0x00 | 0x10 | 0x10 |
|                       | 0xC3 | VPORT_1_SEQ4       |           |           |            | VPORT_1_SEQ3         |                |                |            | 0x00 | 0x10 | 0x10 |
|                       | 0xC4 | VPORT_2_SEQ2       |           |           |            | VPORT_2_SEQ1         |                |                |            | 0x22 | 0x32 | 0x32 |
|                       | 0xC5 | VPORT_2_SEQ4       |           |           |            | VPORT_2_SEQ3         |                |                |            | 0x22 | 0x32 | 0x32 |
|                       | 0xC8 | VPORT_1_CH_OUT_SEL |           |           |            | -RESERVED-           |                |                |            | 0x00 | 0x00 | 0x00 |
|                       | 0xC9 | -RESERVED-         |           |           |            | VPORT_2_CH_OUT_SEL   |                |                |            | 0x00 | 0x00 | 0x00 |
|                       | 0xCA | -RESERVED-         | VCLK_2_EN | VCLK_1_EN | -RESERVED- | -RESERVED-           | VDO_2_EN       | VDO_1_EN       | -RESERVED- | 0x00 | 0xFF | 0xFF |
|                       | 0xCB | -RESERVED-         |           |           |            |                      | OUT_DATA_2_INV | OUT_DATA_1_INV | -RESERVED- | 0x00 | 0x00 | 0x00 |
|                       | 0xCD | VPORT_1_OCLK_SEL   |           |           |            | VPORT_1_OCLK_DLY_SEL |                |                |            | 0x46 | 0x46 | 0x46 |
|                       | 0xCE | VPORT_2_OCLK_SEL   |           |           |            | VPORT_2_OCLK_DLY_SEL |                |                |            | 0x46 | 0x46 | 0x46 |

### 6.1.12 BANK2 Register(0x00~0x1F) : MOTION

| ADDRESS |      | [7]          | [6]        | [5] | [4]            | [3]            | [2]          | [1]            | [0]            | Def. | FHD  | HD   |      |
|---------|------|--------------|------------|-----|----------------|----------------|--------------|----------------|----------------|------|------|------|------|
| B       | 0x00 | -RESERVED-   |            |     |                | CH1_MOTION_PIC |              | -RESERVED-     | CH1_MOTION_OFF | 0x0D | 0xED | 0x09 |      |
|         | 0x01 | CH1_MOD_TSEN |            |     |                |                |              |                |                |      | 0x60 | 0x60 | 0x60 |
|         | 0x02 | -RESERVED-   |            |     |                |                | CH1_MOD_PSEN |                |                |      | 0x23 | 0x88 | 0x88 |
|         | A    | 0x07         | -RESERVED- |     |                | CH2_MOTION_PIC |              | -RESERVED-     | CH2_MOTION_OFF | 0x0D | 0x0D | 0x0D |      |
| N       | 0x08 | CH2_MOD_TSEN |            |     |                |                |              |                |                |      | 0x60 | 0x60 | 0x60 |
| K       | 0x0E | -RESERVED-   |            |     | CH3_MOTION_PIC |                | -RESERVED-   | CH3_MOTION_OFF | 0x0D           | 0x0D | 0x0D |      |      |
| 2       | 0x0F | CH3_MOD_TSEN |            |     |                |                |              |                |                |      | 0x60 | 0x60 | 0x60 |
|         | 0x15 | -RESERVED-   |            |     | CH4_MOTION_PIC |                | -RESERVED-   | CH4_MOTION_OFF | 0x0D           | 0x0D | 0x0D |      |      |
|         | 0x16 | CH4_MOD_TSEN |            |     |                |                |              |                |                |      | 0x60 | 0x60 | 0x60 |

6.1.13 BANK3~4 Register(0x00~0x7F / 0x80~0xFF ) : COAXIAL

| ADDRESS |             | REGISTER NAME |
|---------|-------------|---------------|
| Bank    | Addr        |               |
| 3       | 0x00 ~ 0x7F | Coaxial CH1   |
| 3       | 0x80 ~ 0xFF | Coaxial CH2   |
| 4       | 0x00 ~ 0x7F | Coaxial CH3   |
| 4       | 0x80 ~ 0xFF | Coaxial CH4   |

## 6.1.14 BANK3~4 Register(0x00~0x1F / 0x80~0x9F) : COAXIAL CH1~4

| ADDRESS  |      | [7]                  | [6]        | [5] | [4]                | [3]          | [2] | [1]             | [0]          | Def.           | 30P  | 25P  |      |
|----------|------|----------------------|------------|-----|--------------------|--------------|-----|-----------------|--------------|----------------|------|------|------|
| BANK 3~4 | 0x00 | CH1_BAUD             |            |     |                    |              |     |                 |              | 0x37           | 0x27 | 0x27 |      |
|          | 0x02 | CH1_PELCO_BAUD       |            |     |                    |              |     |                 |              | 0x1B           | 0x1B | 0x1B |      |
|          | 0x03 | CH1_BL_TXST[7:0]     |            |     |                    |              |     |                 |              | 0x05           | 0x0E | 0x0E |      |
|          | 0x04 | CH1_BL_TXST[15:8]    |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |
|          | 0x05 |                      |            |     |                    | CH1_ACT_LEN  |     |                 |              | 0x00           | 0x03 | 0x03 |      |
|          | 0x07 | CH1_PELCO_TXST[7:0]  |            |     |                    |              |     |                 |              | 0x00           | 0x0E | 0x0E |      |
|          | 0x08 | CH1_PELCO_TXST[15:8] |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |
|          | 0x09 |                      |            |     | CH1_COAX_SW_RST    | CH1_CNT_MODE |     |                 | CH1_TX_START | 0x00           | 0x08 | 0x08 |      |
|          | 0x0A |                      |            |     | CH1_TX_BYTE_LENGTH |              |     |                 |              | 0x08           | 0x03 | 0x03 |      |
|          | 0x0B | CH1_PELCO_8BIT       | -RESERVED- |     | CH1_LINE_8BIT      | -RESERVED-   |     | CH1_PACKET_MODE |              | 0x06           | 0x10 | 0x10 |      |
|          | 0x0C |                      |            |     |                    |              |     |                 |              | CH1_PELCO_CTEN | 0x00 | 0x00 | 0x00 |
|          | 0x0D | CH1_BL_HSP[7:0]      |            |     |                    |              |     |                 |              | 0x46           | 0xB4 | 0x48 |      |
|          | 0x0E | CH1_BL_HSP[15:8]     |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x02 |      |
|          | 0x0F |                      |            |     |                    |              |     |                 |              | CH1_PELCO_SHOT | 0x00 | 0x00 | 0x00 |
|          | 0x10 | CH1_TX_DATA_01       |            |     |                    |              |     |                 |              | 0xAA           | 0x00 | 0x00 |      |
|          | 0x11 | CH1_TX_DATA_02       |            |     |                    |              |     |                 |              | 0x1C           | 0x10 | 0x10 |      |
|          | 0x12 | CH1_TX_DATA_03       |            |     |                    |              |     |                 |              | 0x18           | 0x18 | 0x18 |      |
|          | 0x13 | CH1_TX_DATA_04       |            |     |                    |              |     |                 |              | 0xFF           | 0xFF | 0xFF |      |
|          | 0x14 | CH1_TX_DATA_05       |            |     |                    |              |     |                 |              | 0xAA           | 0xAA | 0xAA |      |
|          | 0x15 | CH1_TX_DATA_06       |            |     |                    |              |     |                 |              | 0x3C           | 0x3C | 0x3C |      |
|          | 0x16 | CH1_TX_DATA_07       |            |     |                    |              |     |                 |              | 0xFF           | 0xFF | 0xFF |      |
|          | 0x17 | CH1_TX_DATA_08       |            |     |                    |              |     |                 |              | 0xFF           | 0xFF | 0xFF |      |
|          | 0x18 | CH1_TX_DATA_09       |            |     |                    |              |     |                 |              | 0xAA           | 0xAA | 0xAA |      |
|          | 0x19 | CH1_TX_DATA_10       |            |     |                    |              |     |                 |              | 0x1B           | 0x1B | 0x1B |      |
|          | 0x1A | CH1_TX_DATA_11       |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |
|          | 0x1B | CH1_TX_DATA_12       |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |
|          | 0x1C | CH1_TX_DATA_13       |            |     |                    |              |     |                 |              | 0xAA           | 0xAA | 0xAA |      |
|          | 0x1D | CH1_TX_DATA_14       |            |     |                    |              |     |                 |              | 0x3B           | 0x3B | 0x3B |      |
|          | 0x1E | CH1_TX_DATA_15       |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |
|          | 0x1F | CH1_TX_DATA_16       |            |     |                    |              |     |                 |              | 0x00           | 0x00 | 0x00 |      |



## 6.1.15 BANK3~4 Register(0x20~0x5D / 0xA0~0xDD) : COAXIAL CH1~4

| ADDRESS             | [7]  | [6]                | [5] | [4] | [3] | [2] | [1] | [0] | Def. | 30P  | 25P  |
|---------------------|------|--------------------|-----|-----|-----|-----|-----|-----|------|------|------|
| BANK<br>3<br>/<br>4 | 0x20 | CH1_PELCO_TXDAT_01 |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x21 | CH1_PELCO_TXDAT_02 |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x22 | CH1_PELCO_TXDAT_03 |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x23 | CH1_PELCO_TXDAT_04 |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x2C | CH1_VSO_INV        |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x2D | CH1_HSO_INV        |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x2F | CH1_EVEN_SUM       |     |     |     |     |     |     | 0x01 | 0x00 | 0x00 |
|                     | 0x3A | CH1_CLEAN          |     |     |     |     |     |     | 0x00 | 0x00 | 0x00 |
|                     | 0x50 | CH1_PELCO_8_00     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x51 | CH1_PELCO_8_01     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x52 | CH1_PELCO_8_02     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x53 | CH1_PELCO_8_03     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x54 | CH1_PELCO_8_04     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x55 | CH1_PELCO_8_05     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x56 | CH1_PELCO_8_06     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x57 | CH1_PELCO_8_07     |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x5C | CH1_RX_DONE        |     |     |     |     |     |     | R    | R    | R    |
|                     | 0x5D | CH1_RX_COAX_DUTY   |     |     |     |     |     |     | R    | R    | R    |

## 6.1.16 BANK3~4 Register(0x60~0x7F / 0xE0~0xFF) : COAXIAL CH1~4

| ADDRESS  |      | [7]                   | [6]        | [5] | [4]          | [3] | [2] | [1] | [0]          | Def. | 30P  | 25P  |  |  |  |  |
|----------|------|-----------------------|------------|-----|--------------|-----|-----|-----|--------------|------|------|------|--|--|--|--|
| BANK 3~4 | 0x60 | CH1_DEVICE_ID         |            |     |              |     |     |     |              | 0x00 | 0x48 | 0x48 |  |  |  |  |
|          | 0x62 | CH1_RX_AREA           |            |     |              |     |     |     |              | 0x00 | 0x06 | 0x06 |  |  |  |  |
|          | 0x63 |                       |            |     | CH1_DELAY_ON |     |     |     | CH1_COMM_ON  | 0x00 | 0x01 | 0x01 |  |  |  |  |
|          | 0x64 | CH1_DELAY_CNT         |            |     |              |     |     |     |              | 0x00 | 0x00 | 0x00 |  |  |  |  |
|          | 0x65 |                       |            |     |              |     |     |     | CH1_MSB      | 0x00 | 0x01 | 0x01 |  |  |  |  |
|          | 0x66 | CH1_A_DUTY_ON         | -RESERVED- |     |              |     |     |     |              | 0x00 | 0x80 | 0x80 |  |  |  |  |
|          | 0x67 |                       |            |     |              |     |     |     | CH1_INT_MODE | 0x00 | 0x01 | 0x01 |  |  |  |  |
|          | 0x68 | CH1_RX_SZ             |            |     |              |     |     |     |              | 0x00 | 0x50 | 0x50 |  |  |  |  |
|          | 0x69 | CH1_M_DUTY            |            |     |              |     |     |     |              | 0x00 | 0x00 | 0x00 |  |  |  |  |
|          | 0x6A | CH1_RX_START_POSITION |            |     |              |     |     |     |              | 0x00 | 0x00 | 0x00 |  |  |  |  |
|          | 0x6C | CH1_PELCO16_00 [7:0]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x6D | CH1_PELCO16_00 [15:8] |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x6E | CH1_PELCO16_01 [7:0]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x6F | CH1_PELCO16_01 [15:8] |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x70 | CH1_PELCO16_02[7:0]   |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x71 | CH1_PELCO16_02[15:8]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x72 | CH1_PELCO16_03[7:0]   |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x73 | CH1_PELCO16_03[15:8]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x74 | CH1_PELCO16_04[7:0]   |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x75 | CH1_PELCO16_04[15:8]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x76 | CH1_PELCO16_05[7:0]   |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x77 | CH1_PELCO16_05[15:8]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x78 | CH1_PELCO16_06[7:0]   |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |
|          | 0x79 | CH1_PELCO16_06[15:8]  |            |     |              |     |     |     |              | R    | R    | R    |  |  |  |  |

\* Registers of Bank 5 ~ Bank 10 are not for users.

## 6.2 Register Detail Description

### 6.2.1 VIDEO Registers

#### ● Registers to Power Down Mode

| ADDRESS |      | REGISTER NAME | BITS | VALUE |     | DESCRIPTION                                                                                                                                                                                                                                               |
|---------|------|---------------|------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P |                                                                                                                                                                                                                                                           |
| 0       | 0x00 | PD_VCH1       | [0]  | 0x0   |     | <b>PD_VCH1</b> : Power down for CH1 Video AFE<br><b>PD_VCH2</b> : Power down for CH2 Video AFE<br><b>PD_VCH3</b> : Power down for CH3 Video AFE<br><b>PD_VCH4</b> : Power down for CH4 Video AFE<br><br><b>0</b> : Normal Operation <b>1</b> : Power Down |
|         | 0x01 | PD_VCH2       | [0]  |       |     |                                                                                                                                                                                                                                                           |
|         | 0x02 | PD_VCH3       | [0]  |       |     |                                                                                                                                                                                                                                                           |
|         | 0x03 | PD_VCH4       | [0]  |       |     |                                                                                                                                                                                                                                                           |

#### ● Registers to Control Comb Filter and Video Format

| ADDRESS |      | REGISTER NAME  | BITS  | VALUE                           |                                 | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                   |
|---------|------|----------------|-------|---------------------------------|---------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|
| Bank    | Addr |                |       | 30P                             | 25P                             |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
| 0       | 0x08 | AUTO_1         | [7]   | SD : 0xA0<br>/<br>Others : 0x00 | SD : 0xDD<br>/<br>Others : 0x00 | <b>AUTO_x</b> : A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the Auto_NT_x bit value of the STATUS Register(BANK0, 0xEF) is to be confirmed to distinguish NTSC-M/J and PAL-B/D/G/H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode. (x = channel 1~4 ).<br><br>0 : Auto Detect OFF<br>1 : Auto Detect ON |                                                                                   |
|         | 0x09 | AUTO_2         |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0A | AUTO_3         |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0B | AUTO_4         |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x08 | BSF_MODE_1     | [6:5] |                                 |                                 | <b>BSF_MODE_x</b> : Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~4 )<br><br>00 : LPF Auto Mode<br>10 : Mode 2 (3.5~5.6MHz Cut-off)                                                                                                                                                                                                                                                     | 01 : Mode 1 (2.7~5.4MHz Cut-off)<br>11 : Manual(BANKA~B,0x60 ~ 0x72, 0xD0 ~ 0xE2) |
|         | 0x09 | BSF_MODE_2     |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0A | BSF_MODE_3     |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0B | BSF_MODE_4     |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x08 | VIDEO_FORMAT_1 | [4:0] |                                 |                                 | <b>VIDEO_FORMAT_x</b> : A register to determine the video standards of the input signal (x = channel 1~4 )<br><br>00000 : NTSC-M,J<br>10001 : NTSC-4.43<br>11101 : PAL-B,D,G,H,I<br>10110 : PAL-M<br>11111 : PAL-Nc<br>10101 : PAL-60<br><br>Others : None                                                                                                                                                                                  |                                                                                   |
|         | 0x09 | VIDEO_FORMAT_2 |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0A | VIDEO_FORMAT_3 |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |
|         | 0x0B | VIDEO_FORMAT_4 |       |                                 |                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                   |

● Registers to Control Luminance

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                         |
|---------|------|---------------|-------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                     |
| 0       | 0x0C | BRIGHTNESS_1  | [7:0] | 0xED  | 0xED | <b>BRIGHTNESS_x</b> : Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. (x = channel 1~4 )<br><br>00000001 : + 1                      01111111 : + 127<br>10000000 : - 128                    11111111 : - 1 |
|         | 0x0D | BRIGHTNESS_2  |       |       |      |                                                                                                                                                                                                                                                                                     |
|         | 0x0E | BRIGHTNESS_3  |       |       |      |                                                                                                                                                                                                                                                                                     |
|         | 0x0F | BRIGHTNESS_4  |       |       |      |                                                                                                                                                                                                                                                                                     |

● Registers to Control Contrast

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                         |
|---------|------|---------------|-------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                     |
| 0       | 0x10 | CONTRAST_1    | [7:0] | 0x88  | 0x88 | <b>CONTRAST_x</b> : Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4 )<br><br>00000000 : $\div$ x 0                      01000000 : $\div$ x 0.5<br>10000000 : $\div$ x 1                      11111111 : $\div$ x 2 |
|         | 0x11 | CONTRAST_2    |       |       |      |                                                                                                                                                                                                                                                                                                                                     |
|         | 0x12 | CONTRAST_3    |       |       |      |                                                                                                                                                                                                                                                                                                                                     |
|         | 0x13 | CONTRAST_4    |       |       |      |                                                                                                                                                                                                                                                                                                                                     |

● Registers to Control Sharpness

| ADDRESS |      | REGISTER NAME | BITS  | VALUE                                 |                                                                                                                                                                                                                                       | DESCRIPTION |
|---------|------|---------------|-------|---------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| Bank    | Addr |               |       | 30P                                   | 25P                                                                                                                                                                                                                                   |             |
| 0       | 0x14 | H_SHARPNESS_1 | [7:4] | SD :<br>0x80<br>/<br>Others :<br>0x90 | H_SHARPNESS_x : Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4 )<br><br>0000 : x 0 |             |

● Registers to Control Peaking Filter

| ADDRESS |      | REGISTER NAME | BITS  | VALUE                      |     | DESCRIPTION                                                                                                                                                                                   |
|---------|------|---------------|-------|----------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P                        | 25P |                                                                                                                                                                                               |
| 0       | 0x18 | Y_PEAK_MODE_1 | [7:4] | SD : 0x0<br>/ Others : 0x2 |     | <b>Y_PEAK_MODE_x</b> : Y Peaking Filter control (x = channel 1~4 )<br><br>0000 : 0dB                      0001 : 2dB<br>0010 : 3.5dB                    0011 : 6dB<br>0100 ~ 1111 : Don't use |
|         | 0x19 | Y_PEAK_MODE_2 | [7:4] |                            |     |                                                                                                                                                                                               |
|         | 0x1A | Y_PEAK_MODE_3 | [7:4] |                            |     |                                                                                                                                                                                               |
|         | 0x1B | Y_PEAK_MODE_4 | [7:4] |                            |     |                                                                                                                                                                                               |

- **Registers to Control Low Pass Filter**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE                                                           |     | DESCRIPTION                                                                       |
|---------|------|---------------|-------|-----------------------------------------------------------------|-----|-----------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P                                                             | 25P |                                                                                   |
| 0       | 0x18 | Y_FIR_MODE_1  | [3:0] | SD720H :<br>0x4<br>/<br>SD960H :<br>0x8<br>/<br>Others :<br>0x0 |     | Y_FIR_MODE_x : Y Low Pass Filter control<br>(x = channel 1~4 )                    |
|         | 0x19 | Y_FIR_MODE_2  | [3:0] |                                                                 |     | 0000 : bypass                      0101 : 8MHz                                    |
|         | 0x1A | Y_FIR_MODE_3  | [3:0] |                                                                 |     | 0001 : 6MHz                      0110 : 8.5MHz                                    |
|         | 0x1B | Y_FIR_MODE_4  | [3:0] |                                                                 |     | 0010 : 6.5MHz                  1000 : 9.5MHz                                      |
|         |      |               |       |                                                                 |     | 0011 : 7MHz                      0111 : 9MHz                                      |
|         |      |               |       |                                                                 |     | 0100 : 7.5MHz                  etc : Manual(BANKA~BANKB,<br>0x54~0x5A, 0xD4~0xDA) |

## ● Registers to Control Chrominance

| ADDRESS |      | REGISTER NAME | BITS  | VALUE                                       |           | DESCRIPTION                                                                                                                             |           |                                                                                        |
|---------|------|---------------|-------|---------------------------------------------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------|----------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P                                         | 25P       |                                                                                                                                         |           |                                                                                        |
| 0       | 0x21 | PAL_CM_OFF_1  | [7]   | SD : 0x82<br>SD : 0x02<br><br>Others : 0x92 | SD : 0x02 | PAL_CM_OFF_x (x = channel 1~4)<br>: PAL Compensation On/Off.<br><br>0 : PAL Compensation applied      1 : PAL Compensation not applied. |           |                                                                                        |
|         | 0x25 | PAL_CM_OFF_2  |       |                                             |           |                                                                                                                                         |           |                                                                                        |
|         | 0x29 | PAL_CM_OFF_3  |       |                                             |           |                                                                                                                                         |           |                                                                                        |
|         | 0x2D | PAL_CM_OFF_4  |       |                                             |           |                                                                                                                                         |           |                                                                                        |
|         | 0x21 | IF_FIR_SEL_1  | [6:4] |                                             |           | SD : 0x82<br>SD : 0x02<br><br>Others : 0x92                                                                                             | SD : 0x02 | IF_FIR_SEL_x (x = channel 1~4)<br>: IF Filter drive mode selected.<br><br>000 : bypass |

- **Registers to Control Chrominance**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 0       | 0x22 | COLOROFF_1    | [4]   | 0x0B  | 0x0B | <b>COLOROFF_x</b> (x = channel 1~4)<br>: COLOR OFF<br><br><b>0</b> : Color ON <b>1</b> : Color OFF                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|         | 0x26 | COLOROFF_2    | [4]   |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|         | 0x2A | COLOROFF_3    | [4]   |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|         | 0x2E | COLOROFF_4    | [4]   |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|         | 0x22 | C_KILL_1      | [3:0] |       |      | <b>C_KILL_x[3]</b> (x = channel 1~4)<br>: Select to Color kill mode<br><b>0</b> : Not Y/C separation<br><b>1</b> : Color kill after Y/C separation<br><br><b>C_KILL_x[2:0]</b> (x = channel 1~4)<br>: color kill control.<br><b>000</b> : Burst Amplitude 10% Under & FSC Unlock<br><b>001</b> : Burst Amplitude 5% Under & FSC Unlock<br><b>010</b> : Burst Amplitude 10 % Under<br><b>011</b> : Burst Amplitude 5% Under<br><b>100</b> : Always color on<br><b>101</b> : Always color on.<br><b>110</b> : Always color off<br><b>111</b> : Always color off |
|         | 0x26 | C_KILL_2      |       |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|         | 0x2A | C_KILL_3      |       |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|         | 0x2E | C_KILL_4      |       |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

- Registers to Control Y\_DELAY

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                   |
|---------|------|---------------|-------|-------|------|-----------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                               |
| 0       | 0x30 | Y_DELAY_1     | [4:0] | 0x10  | 0x10 | <b>Y_DELAY_ON_x</b> (x = channel 1~4)<br>: Y DELAY Control, controllable between 0x00 ~ 0x1F. |
|         | 0x31 | Y_DELAY_2     |       |       |      |                                                                                               |
|         | 0x32 | Y_DELAY_3     |       |       |      |                                                                                               |
|         | 0x33 | Y_DELAY_4     |       |       |      |                                                                                               |

- Registers to Control Pedestal and Gamma

| ADDRESS |      | REGISTER NAME | BITS | VALUE |     | DESCRIPTION                                                                                                            |
|---------|------|---------------|------|-------|-----|------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P |                                                                                                                        |
| 0       | 0x34 | PED_ON_1      | [6]  | 0     | 0   | <b>PED_ON_x</b> : Select to Pedestal ON/OFF<br>(x = channel 1~4)<br><br><b>0</b> : Pedestal OFF <b>1</b> : Pedestal ON |
|         | 0x35 | PED_ON_2      |      |       |     |                                                                                                                        |
|         | 0x36 | PED_ON_3      |      |       |     |                                                                                                                        |
|         | 0x37 | PED_ON_4      |      |       |     |                                                                                                                        |

- Registers to Control Chrominance

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                               |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                           |
| 0       | 0x38 | CTI_GAIN_1    | [7:0] | 0x0A  | 0x0A | <b>CTI_GAIN_x[7:6]</b><br>: Adjust CTI Gain Delay                         |
|         | 0x39 | CTI_GAIN_2    |       |       |      |                                                                           |
|         | 0x3A | CTI_GAIN_3    |       |       |      | <b>CTI_GAIN_x[4:0]</b><br>: Adjust gain level for CTI. (x = channel 1~4 ) |
|         | 0x3B | CTI_GAIN_4    |       |       |      | 0x00 : No Gain                      0x01 ~ 0x1F : More larger gain        |

● Registers to Control Chrominance

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                           |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                       |
| 1       | 0x3C | SATURATION_1  | [7:0] | 0x84  | 0x84 | <b>SATURATION_x</b><br>: Color Gain Value (Adjustable up to x2) (x = channel 1~4)<br><br>00000000 : x 0                      10000000 : x 1<br>11000000 : x 1.5                  11111111 : x 2                                       |
|         | 0x3D | SATURATION_2  |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x3E | SATURATION_3  |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x3F | SATURATION_4  |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x40 | HUE_1         | [7:0] | 0x00  | 0x00 | <b>HUE_x</b><br>: Color HUE Control Value (360°/256 per HUE Value 1 unit)<br>(x = channel 1~4)<br><br>00000000 : 0°                      01000000 : 90°<br>10000000 : 180°                  11111111 : 360°                           |
|         | 0x41 | HUE_2         |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x42 | HUE_3         |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x43 | HUE_4         |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x44 | U_GAIN_1      | [7:0] | 0x00  | 0x00 | <b>U_GAIN_x</b><br>: U Gain Value (Adjustable up to x2)<br>(x = channel 1~4)<br><br>00000000 : x 0                      10000000 : x 1<br>11000000 : x 1.5                  11111111 : x 2                                            |
|         | 0x45 | U_GAIN_2      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x46 | U_GAIN_3      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x47 | U_GAIN_4      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x48 | V_GAIN_1      | [7:0] | 0x00  | 0x00 | <b>V_GAIN_x</b><br>: V Gain Value (Adjustable up to x2)<br>(x = channel 1~4)<br><br>00000000 : x 0                      10000000 : x 1<br>11000000 : x 1.5                  11111111 : x 2                                            |
|         | 0x49 | V_GAIN_2      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x4A | V_GAIN_3      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x4B | V_GAIN_4      |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x4C | U_OFFSET_1    | [7:0] | 0x00  | 0x00 | <b>U_OFFSET_x</b><br>: U offset value is adjustable up to ± 7. U offset consists of 2's complements.<br>(x = channel 1~4)<br><br>0001 : +1                              0111 : +7<br>1000 : -8                              1111 : -1 |
|         | 0x4D | U_OFFSET_2    |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x4E | U_OFFSET_3    |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x4F | U_OFFSET_4    |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x50 | V_OFFSET_1    | [7:0] | 0x00  | 0x00 | <b>V_OFFSET_x</b><br>: V offset value is adjustable up to ± 7. V offset consists of 2's complements.<br>(x = channel 1~4)<br><br>0001 : +1                              0111 : +7<br>1000 : -8                              1111 : -1 |
|         | 0x51 | V_OFFSET_2    |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x52 | V_OFFSET_3    |       |       |      |                                                                                                                                                                                                                                       |
|         | 0x53 | V_OFFSET_4    |       |       |      |                                                                                                                                                                                                                                       |

● Registers to Control Field Polarity

| ADDRESS |      | REGISTER NAME | BITS | VALUE |     | DESCRIPTION                                                                                                                 |
|---------|------|---------------|------|-------|-----|-----------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P |                                                                                                                             |
| 0       | 0x54 | FLD_INV_4     | [7]  | 0xF   | 0x0 | <b>FLD_INV_x</b><br>: Field Polarity Control (x = channel 1~4 )<br><br>0 : not Inversion                      1 : Inversion |
|         |      | FLD_INV_3     | [6]  |       |     |                                                                                                                             |
|         |      | FLD_INV_2     | [5]  |       |     |                                                                                                                             |
|         |      | FLD_INV_1     | [4]  |       |     |                                                                                                                             |

● Registers to Insert No Video Information

| ADDRESS |      | REGISTER NAME   | BITS | VALUE |     | DESCRIPTION                                                                                                                                                                         |
|---------|------|-----------------|------|-------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                 |      | 30P   | 25P |                                                                                                                                                                                     |
| 0       | 0x54 | NOVID_INF_IN_14 | [3]  | 0x0   | 0x0 | <b>NOVID_INF_IN_14</b> (x = channel 1~4 )<br>: It can include a NO-Video information at MSB of EAV and SAV.<br><br>0 : No information<br>1 : Put no-video information in EAV or SAV |

● Registers to Control Channel ID

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                        |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                    |
| 0       | 0x54 | CHID_TYPE_14  | [2:0] | 0x1   | 0x1  | CHID_TYPE_x<br>: It determines type of channel ID.(x = channel 1~4 )                               |
|         | 0x55 | CHID_VIN1     | [3:0] | 0x10  | 0x10 | CHID_VIN_x<br>: Register to put CHANNEL ID to distinguish channel. (0x0~0xF)<br>(x = channel 1~4 ) |
|         |      | CHID_VIN2     | [7:4] |       |      |                                                                                                    |
|         | 0x56 | CHID_VIN3     | [3:0] | 0x10  | 0x10 |                                                                                                    |
|         |      | CHID_VIN4     | [7:4] |       |      |                                                                                                    |

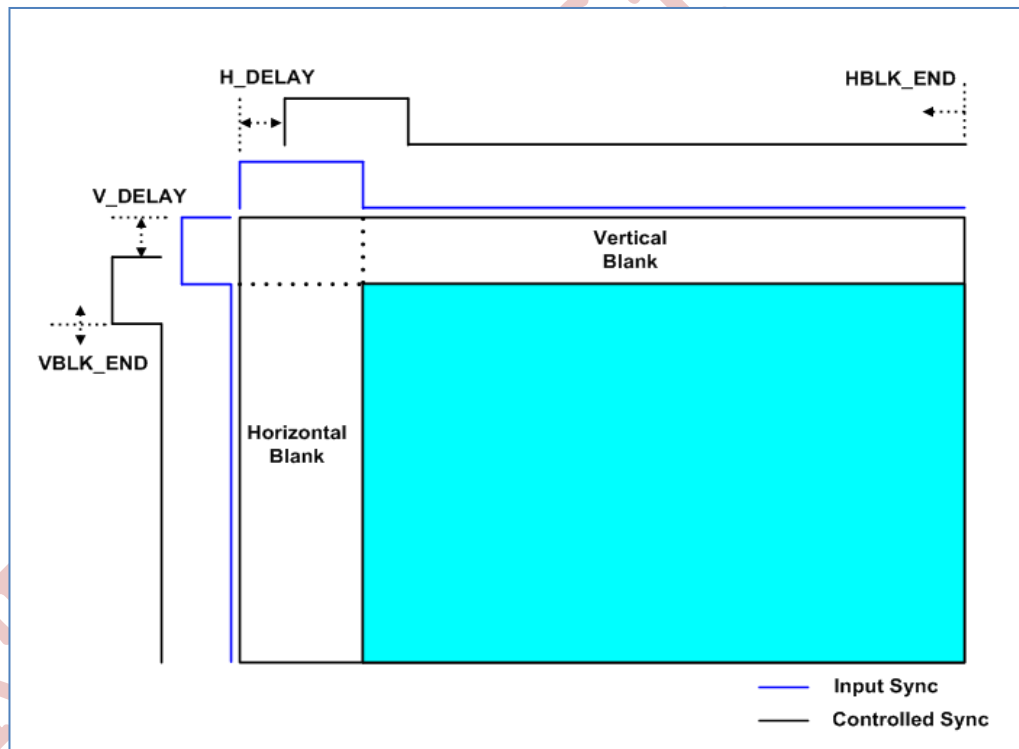
● Registers to Control Video Output Timing

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                        |
|---------|------|---------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                    |
| 0       | 0x58 | H_DELAY_1     | [7:0] | 0x8B  | 0x80 | <b>H_DELAY_x</b><br>: Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~4 )                            |
|         | 0x59 | H_DELAY_2     |       |       |      |                                                                                                                                                                                    |
|         | 0x5A | H_DELAY_3     |       |       |      |                                                                                                                                                                                    |
|         | 0x5B | H_DELAY_4     |       |       |      |                                                                                                                                                                                    |
|         | 0x5C | V_DELAY_1     | [7:0] | 0x9E  | 0x9E | <b>V_DELAY_x[7:6]</b><br>: Select to vblk_str_flg (x = channel 1~4 )<br><b>00 : evenfld    01 : !evenfld    10 : 0    11 : 1</b>                                                   |
|         | 0x5D | V_DELAY_2     |       |       |      | <b>V_DELAY_x[5]</b><br>: V_DELAY_x[4:0] Control Enable (x = channel 1~4 )                                                                                                          |
|         | 0x5E | V_DELAY_3     |       |       |      | <b>V_DELAY_x[4:0] (When V_DELAY_x[5] = 1)</b><br>: Register to determine the Vertical start position of output image to Vsync extracted in analog input signal. (x = channel 1~4 ) |
|         | 0x5F | V_DELAY_4     |       |       |      |                                                                                                                                                                                    |



● Registers to Control Video Output Timing

| ADDRESS |      | REGISTER NAME | BITS  | VALUE              |                    | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|------|---------------|-------|--------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P                | 25P                |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0       | 0x60 | HBLK_END_1    | [7:0] | 0x00               | 0x00               | <b>HBLK_END_x</b><br>: Register to control Width of Horizontal Blanking. If user increments or decrements the value of this register, then the Active region is changed.<br>(x = channel 1~4 )                                                                                                                                                                                                                                                     |
|         | 0x61 | HBLK_END_2    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x62 | HBLK_END_3    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x63 | HBLK_END_4    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x64 | VBLK_END_1    | [7:0] | 0xC0<br>SD<br>0x28 | 0xC0<br>SD<br>0x2D | <b>VBLK_END_x[7:6]</b><br>: Select to vblk_end_fld (x = channel 1~4 )<br>00 : evenfld    01 : !evenfld    10 : 0    11 : 1<br><br><b>VBLK_END_x[5]</b><br>: VBLK_END_x[4:0] Control Enable<br>(x = channel 1~4 )<br><br><b>VBLK_END_x[4:0] (When VBLK_END_x[5] = 1)</b><br>: Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed.<br>(x = channel 1~4 ) |
|         | 0x65 | VBLK_END_2    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x66 | VBLK_END_3    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x67 | VBLK_END_4    |       |                    |                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |



● Registers to Control Video Output Timing

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                            |
| 0       | 0x68 | H_CROP_S_1    | [7:0] | 0x00  | 0x00 | H_CROP_S_x : Adjust the horizontal crop start point.<br>(x = channel 1~4 ) |
|         | 0x69 | H_CROP_S_2    |       |       |      |                                                                            |
|         | 0x6A | H_CROP_S_3    |       |       |      |                                                                            |
|         | 0x6B | H_CROP_S_4    |       |       |      |                                                                            |
|         | 0x6C | H_CROP_E_1    | [7:0] | 0x00  | 0x00 | H_CROP_E_x : Adjust the horizontal crop end point.<br>(x = channel 1~4 )   |
|         | 0x6D | H_CROP_E_2    |       |       |      |                                                                            |
|         | 0x6E | H_CROP_E_3    |       |       |      |                                                                            |
|         | 0x6F | H_CROP_E_4    |       |       |      |                                                                            |
|         | 0x70 | V_CROP_S_1    | [7:0] | 0x00  | 0x00 | V_CROP_S_x : Adjust the vertical crop start point.<br>(x = channel 1~4 )   |
|         | 0x71 | V_CROP_S_2    |       |       |      |                                                                            |
|         | 0x72 | V_CROP_S_3    |       |       |      |                                                                            |
|         | 0x73 | V_CROP_S_4    |       |       |      |                                                                            |
|         | 0x74 | V_CROP_E_1    | [7:0] | 0x00  | 0x00 | V_CROP_E_x : Adjust the vertical crop end point.<br>(x = channel 1~4 )     |
|         | 0x75 | V_CROP_E_2    |       |       |      |                                                                            |
|         | 0x76 | V_CROP_E_3    |       |       |      |                                                                            |
|         | 0x77 | V_CROP_E_4    |       |       |      |                                                                            |

● Registers to Control Back Ground Color

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------|------|---------------|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 0       | 0x78 | BGDCOL_1      | [3:0] | 0x88  | 0x88 | <b>BGDCOL_x</b><br>: When No-Video, BackGround Color is used. (x = channel 1~4 )<br><br>0000 : Blue<br>0001 : White (75%)<br>0010 : Yellow<br>0011 : Cyan<br>0100 : Green<br>0101 : Magenta<br>0110 : Red<br>0111 : Blue<br>1000 : Black<br>1001 : Gray<br>1010 : Red (NEXTCHIP)<br>1011 : Yellow (NEXTCHIP)<br>1100 : Magenta (NEXTCHIP)<br>1101 : Green (NEXTCHIP)<br>1110 : Blue (NEXTCHIP)<br>1111 : Cyan (NEXTCHIP)<br>* These color information is exactly same as controllers provided by NEXTCHIP |
|         |      | BGDCOL_2      | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         | 0x79 | BGDCOL_3      | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|         |      | BGDCOL_4      | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

● Registers to Control Data Out Mode

| ADDRESS |      | REGISTER NAME   | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|---------|------|-----------------|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                 |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 0       | 0x7A | DATA_OUT_MODE_1 | [3:0] | 0x11  | 0x11 | <b>DATA_OUT_MODE_x</b><br>: It limits a level of output data, can change signals of Cb and Cr each.<br>(x = channel 1~4 )<br><br>0000 : Y(016~235), Cb(016~240), Cr(016~240)<br>0001 : Y(001~254), Cb(001~254), Cr(001~254)<br>0010 : Y(000~255), Cb(000~255), Cr(000~255)<br>0011 : Cb / Cr Change, 016~235<br>0100 : Cb / Cr Change, 001~254<br>0101 : Cb / Cr Kill, 016~235<br>0110 : Cb / Cr Kill, 001~254<br>Others : Background color output |
|         |      | DATA_OUT_MODE_2 | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         | 0x7B | DATA_OUT_MODE_3 | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|         |      | DATA_OUT_MODE_4 | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

- **Registers For Each Channel Control**

- **Registers to Select AHD Mode**

- **Registers to Control H\_DELAY**

- **Registers to Control Horizontal ZOOM**



● Registers to Control Y/C DELAY

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                          |
|---------|------|---------------|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                      |
| 0       | 0xA0 | DF_YDELAY_4   | [3:0] | 0x00  | 0x00 | <b>DF_YDELAY_x</b> ( x = channel 1~4 )<br>: Y(Luminance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF.   |
|         | 0xA1 | DF_YDELAY_3   |       |       |      |                                                                                                                                      |
|         | 0xA2 | DF_YDELAY_2   |       |       |      |                                                                                                                                      |
|         | 0xA3 | DF_YDELAY_1   |       |       |      |                                                                                                                                      |
|         | 0xA0 | DF_CDELAY_4   | [7:4] | 0x00  | 0x00 | <b>DF_CDELAY_x</b> ( x = channel 1~4 )<br>: C(Chrominance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF. |
|         | 0xA1 | DF_CDELAY_3   |       |       |      |                                                                                                                                      |
|         | 0xA2 | DF_CDELAY_2   |       |       |      |                                                                                                                                      |
|         | 0xA3 | DF_CDELAY_1   |       |       |      |                                                                                                                                      |

- **Registers to Status Registers (Read Only)**

## ● Registers to Status Registers (Read Only)

2016.10.12 (REV 1.0)

● Registers to Interrupt clear for Status Registers

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                        |
|---------|------|---------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                                    |
| 0       | 0xB0 | NOVID_01B     | [0]  | Read  | Read | <b>NOVID_0xB</b><br>: Each Channel Video Decoder No Video detection Status with HOLD option<br>(x = Channel number)<br><br><b>0</b> : On Video <b>1</b> : No Video |
|         |      | NOVID_02B     | [1]  |       |      |                                                                                                                                                                    |
|         |      | NOVID_03B     | [2]  |       |      |                                                                                                                                                                    |
|         |      | NOVID_04B     | [3]  |       |      |                                                                                                                                                                    |
|         | 0xB1 | MOTION_01B    | [0]  | Read  | Read | <b>MOTION_0xB</b><br>: Each Channel Motion detection Status with HOLD option<br>(x = Channel number)<br><br><b>0</b> : No MOTION <b>1</b> : On MOTION              |
|         |      | MOTION_02B    | [1]  |       |      |                                                                                                                                                                    |
|         |      | MOTION_03B    | [2]  |       |      |                                                                                                                                                                    |
|         |      | MOTION_04B    | [3]  |       |      |                                                                                                                                                                    |

● Registers to Interrupt clear for Status Registers

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                   |
|---------|------|---------------|------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                               |
| 0       | 0xB4 | MUTE_01B      | [0]  | Read  | Read | <b>MUTE_0xB</b><br>: Each Channel MUTE detection Status with HOLD option<br>(x = Channel number)<br><br><b>0</b> : On Audio<br><br><b>1</b> : No Audio (MUTE) |
|         |      | MUTE_02B      | [1]  |       |      |                                                                                                                                                               |
|         |      | MUTE_03B      | [2]  |       |      |                                                                                                                                                               |
|         |      | MUTE_04B      | [3]  |       |      |                                                                                                                                                               |
|         |      | MUTE_05B      | [4]  |       |      |                                                                                                                                                               |
|         |      | MUTE_06B      | [5]  |       |      |                                                                                                                                                               |
|         |      | MUTE_07B      | [6]  |       |      |                                                                                                                                                               |
|         |      | MUTE_08B      | [7]  |       |      |                                                                                                                                                               |
|         | 0xB5 | MUTE_09B      | [0]  | Read  | Read |                                                                                                                                                               |
|         |      | MUTE_10B      | [1]  |       |      |                                                                                                                                                               |
|         |      | MUTE_11B      | [2]  |       |      |                                                                                                                                                               |
|         |      | MUTE_12B      | [3]  |       |      |                                                                                                                                                               |
|         |      | MUTE_13B      | [4]  |       |      |                                                                                                                                                               |
|         |      | MUTE_14B      | [5]  |       |      |                                                                                                                                                               |
|         |      | MUTE_15B      | [6]  |       |      |                                                                                                                                                               |
|         |      | MUTE_16B      | [7]  |       |      |                                                                                                                                                               |
|         | 0xB6 | MUTEMIC_01B   | [0]  | Read  | Read | <b>MUTEMIC_01~02B</b><br>: Each Internal and External Mic 2 Channel MUTE detection Status<br><br><b>0</b> : On Audio<br><b>1</b> : No Audio (MUTE)            |
|         |      | MUTEMIC_02B   | [1]  |       |      |                                                                                                                                                               |

● Registers to Interrupt clear for Status Registers

| ADDRESS |      | REGISTER NAME   | BITS | VALUE |      | DESCRIPTION                                                                                                                                            |
|---------|------|-----------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                 |      | 30P   | 25P  |                                                                                                                                                        |
| 1       | 0xB7 | COAX_RX_DONE_1B | [0]  | Read  | Read | <b>COAX_RX_DONE_x</b><br>: COAXIAL_RX_Detecting Checking Status (x = channel number)<br><br><b>0</b> : No Detecting<br><b>1</b> : COAXIAL_RX_Detecting |
|         |      | COAX_RX_DONE_2B | [1]  |       |      |                                                                                                                                                        |
|         |      | COAX_RX_DONE_3B | [2]  |       |      |                                                                                                                                                        |
|         |      | COAX_RX_DONE_4B | [3]  |       |      |                                                                                                                                                        |

- **Registers to Interrupt clear for Status Registers**

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                                                                                |
|---------|------|---------------|------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                                                                                            |
| 0       | 0xB8 | RD_STATE_CLR  | [7]  | 0x90  | 0x90 | <b>RD_STATE_CLR</b><br>: Interrupt clear condition selection<br><br><b>0</b> : Interrupt clear when BANK0, 0xC0~0xC6 Addr Register Read<br><b>1</b> : Interrupt clear when BANK0, 0xB8~0xBE / 0xC0~0xC6 Addr Register Read |
|         |      | STATE_HOLD    | [4]  |       |      | <b>STATE_HOLD</b><br>: Interrupt Hold condition selection<br><br><b>0</b> : No Hold Option, State is Real Time update.<br><b>1</b> : Hold Option operation. State is Hold until cleared                                    |

- **Registers to Control IRQ**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------|------|---------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 0       | 0xB9 | IRQ_MSB       | [4]   | 0x00  | 0x00 | <b>IRQ_MSB</b><br>: Control output data of IRQ pin<br><b>0</b> : 1 item output for MPP signal<br><b>1</b> : 2~5 item OR output for MPP signal                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|         |      | IRQ_INV       | [3]   |       |      | <b>IRQ_INV</b><br>: IRQ pin output signal inversion<br><b>0</b> : Not Inversion <b>1</b> : Inversion                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|         |      | IRQ_SEL       | [2:0] |       |      | <b>IRQ_SEL</b><br>: Select IRQ pin output signals selection<br>When IRQ_MSB(BANK1,0xB9[4]) = 0,<br><b>0</b> : <b>0 (Zero)</b><br><b>1</b> : interrupt request by the No video detection<br><b>2</b> : interrupt request by the Mute detection<br><b>3</b> : interrupt request by the Motion detection<br><b>4</b> : interrupt request by the Black detection<br><b>5</b> : interrupt request by the White detection<br><b>6</b> : ALINKO<br><b>7</b> : BNCO<br>When IRQ_MSB(BANK1,0xB9[4]) = 1,<br><b>0</b> : Novid   Motion interrupt request<br><b>1</b> : Novid   Black interrupt request<br><b>2</b> : Novid   White interrupt request<br><b>3</b> : Black   White interrupt request<br><b>4</b> : Black   Motion interrupt request<br><b>5</b> : White   Motion interrupt request<br><b>6</b> : Novid   Motion   Black interrupt request<br><b>7</b> : Black   White   Motion interrupt request |



● Registers to Show Locking Status (Read Only)

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                       |
|---------|------|---------------|------|-------|------|-------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                   |
| 0       | 0xE0 | AGC_LOCK_04   | [3]  | Read  | Read | <b>AGC_LOCK_0x</b><br>: Video AGC Locking Status ( x = channel number )<br><br>0 : No Locking<br>1 : Locking      |
|         |      | AGC_LOCK_03   | [2]  |       |      |                                                                                                                   |
|         |      | AGC_LOCK_02   | [1]  |       |      |                                                                                                                   |
|         |      | AGC_LOCK_01   | [0]  |       |      |                                                                                                                   |
|         | 0xE1 | CMP_LOCK_04   | [3]  | Read  | Read | <b>CMP_LOCK_0x</b><br>: Video CLAMP Locking status ( x = channel number )<br><br>0 : No Locking<br>1 : Locking    |
|         |      | CMP_LOCK_03   | [2]  |       |      |                                                                                                                   |
|         |      | CMP_LOCK_02   | [1]  |       |      |                                                                                                                   |
|         |      | CMP_LOCK_01   | [0]  |       |      |                                                                                                                   |
|         | 0xE2 | H_LOCK_04     | [3]  | Read  | Read | <b>H_LOCK_0x</b><br>: Video Horizontal Locking status ( x = channel number )<br><br>0 : No Locking<br>1 : Locking |
|         |      | H_LOCK_03     | [2]  |       |      |                                                                                                                   |
|         |      | H_LOCK_02     | [1]  |       |      |                                                                                                                   |
|         |      | H_LOCK_01     | [0]  |       |      |                                                                                                                   |

● Registers to Show Chip Status (Read Only)

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                         |
|---------|------|---------------|------|-------|------|-----------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                     |
| 0       | 0xE7 | BW_04         | [3]  | Read  | Read | <b>BW_0x</b><br>: Black / White Detection status ( x = channel number )<br><br>0 : Color<br>1 : B/W |
|         |      | BW_03         | [2]  |       |      |                                                                                                     |
|         |      | BW_02         | [1]  |       |      |                                                                                                     |
|         |      | BW_01         | [0]  |       |      |                                                                                                     |

● Registers to read the FSC Status (Read Only)

| ADDRESS |      | REGISTER NAME    | BITS | VALUE |      | DESCRIPTION                                                                                                                                      |
|---------|------|------------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                  |      | 30P   | 25P  |                                                                                                                                                  |
| 0       | 0xE8 | FSC_CHG_DONE_01  | [3]  | Read  | Read | <b>FSC_CHG_DONE_x</b><br>: A status which FSC changed done or not ( x = channel number )<br><br>0 : not changed                      1 : changed |
|         | 0xE9 | FSC_CHG_DONE_02  |      |       |      |                                                                                                                                                  |
|         | 0xEA | FSC_CHG_DONE_03  |      |       |      |                                                                                                                                                  |
|         | 0xEB | FSC_CHG_DONE_04  |      |       |      |                                                                                                                                                  |
|         | 0xE8 | CKILL_01         | [2]  | Read  | Read | <b>CKILL_x</b><br>: color kill status                      ( x = channel number )<br><br>0 : Color On                              1 : Color Off |
|         | 0xE9 | CKILL_02         |      |       |      |                                                                                                                                                  |
|         | 0xEA | CKILL_03         |      |       |      |                                                                                                                                                  |
|         | 0xEB | CKILL_04         |      |       |      |                                                                                                                                                  |
|         | 0xE8 | FSC_LOCK_DONE_01 | [1]  | Read  | Read | <b>FSC_LOCK_DONE_x</b><br>: FSC LOCK Detection Status ( x = channel number )                                                                     |
|         | 0xE9 | FSC_LOCK_DONE_02 |      |       |      |                                                                                                                                                  |
|         | 0xEA | FSC_LOCK_DONE_03 |      |       |      |                                                                                                                                                  |
|         | 0xEB | FSC_LOCK_DONE_04 |      |       |      |                                                                                                                                                  |
|         | 0xE8 | NOVIDEO_01       | [0]  | Read  | Read | <b>NOVIDEO_x</b><br>: NOVIDEO Status (x=channel number)                                                                                          |
|         | 0xE9 | NOVIDEO_02       |      |       |      |                                                                                                                                                  |
|         | 0xEA | NOVIDEO_03       |      |       |      |                                                                                                                                                  |
|         | 0xEB | NOVIDEO_04       |      |       |      |                                                                                                                                                  |

● Registers to Show Chip Status (Read Only)

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                              |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                          |
| 0       | 0xF4 | DEV_ID        | [7:0] | Read  | Read | <b>DEV_ID</b><br>: It shows Device ID (NVP6134C = 0x90 ) |
|         | 0xF5 | REV_ID        | [7:0] | Read  | Read | <b>REV_ID</b><br>: It shows Revision ID (0x01)           |

## 6.2.4 AUDIO Registers

### ● Registers to Control Audio AFE and DFE

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                 |
|---------|------|---------------|------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                                                                                                             |
| 1       | 0x00 | PD_AU_AFE     | [7]  | 0x02  | 0x02 | <b>PD_AU_AFE</b><br>: Audio AFE LIVE CH1~CH4 and MIC1 Power Down Mode selection<br>0 : Operation<br>1 : Power Down                                                                                                                          |
|         |      | PD_AU_DAC     | [6]  |       |      | <b>PD_AU_DAC</b><br>: Audio DAC Power Down Mode selection<br>0 : Operation<br>1 : Power Down                                                                                                                                                |
|         |      | RM_PB_PIN     | [3]  |       |      | <b>RM_PB_PIN</b><br>: Selection of clock and sync for ADATA_REC, ADATA_SP pin<br>0 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_REC, ADATA_SP pin<br>1 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_REC, ADATA_SP pin |
|         |      | PB_RM_PIN     | [2]  |       |      | <b>PB_RM_PIN</b><br>: Selection of clock and sync for ADATA_PB pin<br>0 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_PB,<br>1 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_PB,                                        |
|         |      | FILTER_ON     | [1]  |       |      | <b>FILTER_ON</b><br>: Set ADC sampling rate<br>0 : Non-oversample (16KHz)<br>1 : Oversample (64KHz)                                                                                                                                         |
|         |      | EN_32K_MODE   | [0]  |       |      | <b>EN_32K_MODE</b><br>: Operate whole audio system as 32K mode<br>0 : 16K Mode<br>1 : 32K Mode                                                                                                                                              |

### ● Registers to Control Audio Input Gain

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                             |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                         |
| 1       | 0x01 | AIGAIN_01     | [7:0] | 0x08  | 0x08 | AIGAIN_x / MIGAIN_x<br>: The gain of analog audio input AIN1-8 and MICIN1                               |
|         | 0x02 | AIGAIN_02     | [7:0] |       |      | 0000 : mute0001 : 0.125<br>0010 : 0.250011 : 0.375<br>0100 : 0.50101 : 0.625<br>0110 : 0.750111 : 0.875 |
|         | 0x03 | AIGAIN_03     | [7:0] |       |      | 1000 : 1.01001 : 1.125<br>1010 : 1.251011 : 1.375<br>1100 : 1.51101 : 1.625                             |
|         | 0x04 | AIGAIN_04     | [7:0] |       |      | 1110 : 1.751111 : 1.875<br>10000 : 2.010001 : 2.125                                                     |
|         | 0x05 | MIGAIN_01     | [3:0] |       |      | 10000 ~ 11111111 : step by about 0.125                                                                  |
|         |      |               |       |       |      |                                                                                                         |

● Registers to Audio Interface

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                |
|---------|------|---------------|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                            |
| 1       | 0x06 | CAS_PB        | [7]   | 0x3B  | 0x3B | <b>CAS_PB</b><br>: The Usage of Playback Data when Cascade Mode<br>0 : use multiple playback data, received through all stage<br>1 : use single playback data, received through last stage |
|         |      | TRANS_MODE    | [6]   |       |      | <b>TRANS_MODE</b><br>: Control the phase between transferred clock and cascade data<br>0 : Same phase                      1 : Inverted phase                                              |
|         |      | CAS_4CH       | [5]   |       |      | <b>CAS_4CH</b><br>: Channel number of 1-chip for Audio Cascade.<br>0 : 8 Channels                      1 : 4 Channels                                                                      |
|         |      | CAS_PIN       | [4]   |       |      | <b>CAS_PIN</b><br>: Control the usage of ADATA_CASI and ADATA_CASO as cascade transmitting<br>0 : Don't Use                      1 : Use                                                   |
|         |      | CASCADE_MODE  | [3]   |       |      | <b>CASCADE_MODE</b><br>: Set the chip position when it is cascaded.<br>0 : ACLK/ASYNC/ADATA Use      1 : ALINKI/ALINKO Use                                                                 |
|         |      | CHIP_STAGE    | [1:0] |       |      | <b>CHIP_STAGE</b><br>: Selection of chip state for cascade<br>0 : middle stage                      1 : last stage<br>2 : first stage                      3 : single chip operation       |
|         | 0x07 | RM_MASTER     | [7]   | 0xC8  | 0xC8 | <b>RM_MASTER</b><br>: Selection of master & slave mode of ACLK_REC and ASYNC_REC<br>0 : Slave mode operation      1 : Master mode operation                                                |
|         |      | RM_CLK        | [6]   |       |      | <b>RM_CLK</b><br>: Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC<br>0 : inverted clock                      1 : non-inverted clock      |
|         |      | RM_BITRATE    | [5:4] |       |      | <b>RM_BITRATE</b><br>: Set the bit rate of audio signal outputted to ADATA_REC<br>0 : 256fs                      1 : 384fs<br>2 : 320fs                      3 : Don't Use                 |
|         |      | RM_SAMRATE    | [3]   |       |      | <b>RM_SAMRATE</b><br>: Set the sampling rate of data outputted to ADATA_REC<br>0 : 8KHz                      1 : 16KHz                                                                     |
|         |      | RM_BITWID     | [2]   |       |      | <b>RM_BITWID</b><br>: Set the bit width of data outputted to ADATA_REC<br>0 : 16bits                      1 : 8bits                                                                        |
|         |      | RM_SSP        | [1]   |       |      | <b>RM_SSP</b><br>: Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode.<br>0 : DSP mode                      1 : SSP mode                                     |
|         |      | RM_SYNC       | [0]   |       |      | <b>RM_SYNC</b><br>: Set the sync's mode inputted/outputted to ASYNC_REC.<br>0 : I2S mode                      1 : DSP mode                                                                 |

● Registers to Control Audio interface

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                   |
|---------|------|---------------|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                               |
| 1       | 0x08 | RM_BIT_SWAP   | [7]   | 0x03  | 0x03 | <b>RM_BIT_SWAP</b><br>: Set the bit sequence of Audio Data for ADATA_REC<br><br>0 : MSB first                      1 : LSB first                                                              |
|         |      | RM_LAW_SEL    | [6]   |       |      | <b>RM_LAW_SEL</b><br>: Define the G.711 data format outputted to ADATA_REC<br><br>0 : u-law                              1 : a-law                                                            |
|         |      | RM_FORMAT     | [5:4] |       |      | <b>RM_FORMAT</b><br>: Define the data format outputted to ADATA_REC<br><br>0 : linear PCM                      1 : Unsigned linear PCM<br>2 : G.711 format                      3 : Don't Use |
|         |      | R_ADATSP      | [2]   |       |      | <b>R_ADATSP</b><br>: Selection of output data for ADATA_SP<br><br>0 : Speaker data                      1 : Record data                                                                       |
|         |      | R_MULTCH      | [1:0] |       |      | <b>R_MULTCH</b><br>: Selection of number of Channel for ADATA_REC<br><br>0 : 2ch                                  1 : 4ch<br>2 : 8ch                                  3 : 16ch                |

● Registers to Control Audio Interface

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|---------|------|---------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 1       | 0x09 | R_SEQ_01[4]   | [0]   | 0x0   | 0x0  | R_SEQ<br>: Sequence of Audio Data for ADATA_REC<br><br>00000 : channel 1 data<br>00001 : channel 2 data<br>00010 : channel 3 data<br>00011 : channel 4 data<br>00100 : channel 5 data<br>00101 : channel 6 data<br>00110 : channel 7 data<br>00111 : channel 8 data<br>01000 : channel 9 data<br>01001 : channel 10 data<br>01010 : channel 11 data<br>01011 : channel 12 data<br>01100 : channel 13 data<br>01101 : channel 14 data<br>01110 : channel 15 data<br>01111 : channel 16 data<br>10000 : Mic input 1<br>10001 : Mic input 2 |
|         |      | R_SEQ_02[4]   | [1]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_03[4]   | [2]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_04[4]   | [3]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_05[4]   | [4]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_06[4]   | [5]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_07[4]   | [6]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_08[4]   | [7]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         | 0x0A | R_SEQ_01[3:0] | [3:0] | 0x10  | 0x10 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_02[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         | 0x0B | R_SEQ_03[3:0] | [3:0] | 0x32  | 0x32 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_04[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         | 0x0C | R_SEQ_05[3:0] | [3:0] | 0x54  | 0x54 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_06[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         | 0x0D | R_SEQ_07[3:0] | [3:0] | 0x76  | 0x76 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|         |      | R_SEQ_08[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

## ● Registers to Control Audio Interface

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 1       | 0x0E | R_SEQ_09[4]   | [0]   | 0x0   | 0x0  | <b>R_SEQ_xx / MIC_SEQ_0x.</b> (x = channel number)<br>: Sequence of Audio Data for ADATA_REC<br><br>00000 : channel 1 data<br>00001 : channel 2 data<br>00010 : channel 3 data<br>00011 : channel 4 data<br>00100 : channel 5 data<br>00101 : channel 6 data<br>00110 : channel 7 data<br>00111 : channel 8 data<br>01000 : channel 9 data<br>01001 : channel 10 data<br>01010 : channel 11 data<br>01011 : channel 12 data<br>01100 : channel 13 data<br>01101 : channel 14 data<br>01110 : channel 15 data<br>01111 : channel 16 data<br>10000 : Mic input 1<br>10001 : Mic input 2 |
|         |      | R_SEQ_10[4]   | [1]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_11[4]   | [2]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_12[4]   | [3]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_13[4]   | [4]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_14[4]   | [5]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_15[4]   | [6]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_16[4]   | [7]   | 0x0   | 0x0  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x0F | R_SEQ_09[3:0] | [3:0] | 0x98  | 0x98 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_10[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x10 | R_SEQ_11[3:0] | [3:0] | 0xBA  | 0xBA |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_12[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x11 | R_SEQ_13[3:0] | [3:0] | 0xDC  | 0xDC |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_14[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x12 | R_SEQ_15[3:0] | [3:0] | 0xFE  | 0xFE |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         |      | R_SEQ_16[3:0] | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x3C | MIC_SEQ_01    | [4:0] | 0x10  | 0x10 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|         | 0x3D | MIC_SEQ_02    | [4:0] | 0x11  | 0x11 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

- **Registers to Control Audio Interface**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                         |
|---------|------|---------------|-------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                     |
| 1       | 0x13 | PB_MASTER     | [7]   | 0x08  | 0x08 | <b>PB_MASTER</b><br>: Selection of master & slave mode of ACLK_PB and ASYNC_PB<br><br>0 : Slave mode                      1 : Master mode                                           |
|         |      | PB_CLK        | [6]   |       |      | <b>PB_CLK</b><br>: Set the relationship between audio signal outputted to ADATA_PB and clock outputted to ACLK_PB<br><br>0 : inverted clock                  1 : non-inverted clock |
|         |      | PB_BITRATE    | [5:4] |       |      | <b>PB_BITRATE</b><br>: Set the bit rate of audio signal outputted to ADATA_PB<br><br>0 : 256fs                              1 : 384fs<br>2 : 320fs                                  |
|         |      | PB_SAMRATE    | [3]   |       |      | <b>PB_SAMRATE</b><br>: Set the sampling rate of data outputted to ADATA_PB<br><br>0 : 8KHz                                1 : 16KHz                                                 |
|         |      | PB_BITWID     | [2]   |       |      | <b>PB_BITWID</b><br>: Set the bit width of data outputted to ADATA_PB<br><br>0 : 16bits                              1 : 8bits                                                      |
|         |      | PB_SSP        | [1]   |       |      | <b>PB_SSP</b><br>: Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode.<br><br>0 : DSP mode                         1 : SSP mode              |
|         |      | PB_SYNC       | [0]   |       |      | <b>PB_SYNC</b><br>: Set the sync's mode inputted/outputted to ASYNC_PB.<br><br>0 : I2S mode                         1 : DSP mode                                                    |

## ● Registers to Control Audio Interface

| <b>ADDRESS</b> |             | <b>REGISTER NAME</b> | <b>BITS</b> | <b>VALUE</b> |            | <b>DESCRIPTION</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|----------------|-------------|----------------------|-------------|--------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Bank</b>    | <b>Addr</b> |                      |             | <b>30P</b>   | <b>25P</b> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| <b>1</b>       | <b>0x14</b> | PB_BIT_SWAP          | [7]         | 0x00         | 0x00       | <b>PB_BIT_SWAP</b><br>: Set the bit sequence of Audio Data for ADATA_PB<br><br><div style="text-align: center;"> <span>0    :</span> MSB first               <span style="margin-left: 6em;"><b>1    :</b> LSB first</span> </div>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|                |             | PB_SEL               | [4:0]       |              |            | <b>PB_SEL</b><br>: select the audio input channel for playback input<br><br><div style="display: flex; justify-content: space-between;"> <div>             00    : channel 01<br/>             02    : channel 03<br/>             04    : channel 05<br/>             06    : channel 07<br/>             08    : channel 09<br/>             0A    : channel 11<br/>             0C    : channel 13<br/>             0E    : channel 15<br/>             10    : Mic input 1           </div> <div>             01    : channel 02<br/>             03    : channel 04<br/>             05    : channel 06<br/>             07    : channel 08<br/>             09    : channel 10<br/>             0B    : channel 12<br/>             0D    : channel 14<br/>             0F    : channel 16<br/>             11    : Mic input 2           </div> </div> |

- **Registers to Control Audio Interface**

[illegible]

## ● Registers to Control Audio Mixing Gain

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------|------|---------------|-------|-------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 1       | 0x16 | MIX_RATIO_01  | [3:0] | 0x88  | 0x88 | <b>MIX_RATIO_x</b><br>: Set the mixing gain for AIN1-15. ( x = channel number )<br><br><div><div>0 : mute</div><div>2 : 0.31</div><div>4 : 0.5</div><div>6 : 0.75</div><div>8 : 1.0</div><div>10 : 1.5</div><div>12 : 2.0</div><div>14 : 2.5</div><div>1 : 0.25</div><div>3 : 0.38</div><div>5 : 0.63</div><div>7 : 0.88</div><div>9 : 1.25</div><div>11 : 1.75</div><div>13 : 2.25</div><div>15 : 2.75</div></div> |
|         |      | MIX_RATIO_02  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x17 | MIX_RATIO_03  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_04  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x18 | MIX_RATIO_05  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_06  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x19 | MIX_RATIO_07  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_08  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_09  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x1A | MIX_RATIO_10  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_11  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x1B | MIX_RATIO_12  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_13  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x1C | MIX_RATIO_14  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         |      | MIX_RATIO_15  | [3:0] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |
|         | 0x1D | MIX_RATIO_16  | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                     |

- **Registers to Control Audio Mixing Gain**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                  |
|---------|------|---------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                              |
| 1       | 0x1E | MIX_RATIO_M1  | [3:0] | 0x88  | 0x88 | <b>MIX_RATIO_Mx/ MIX_RATIO_Px</b><br>: Set the mixing gain for MICIN1~2 / PBIN1~4. ( x =    channel number )<br><br>0 : mute |

- **Registers to Control Audio Mixing Output Mode**

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------|------|---------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1       | 0x23 | MIX_DERATIO   | [5]   | 0x19  | 0x19 | <b>MIX_DERATIO</b><br>: Selection of the mixing gain mode<br><br>0 : Apply the mixing gain for MIX_RATIO_01-P4 (BANK1_0x16~0x21 Addr) separately<br>1 : Apply all mixing gain as the same gain (x1).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|         |      | MIX_OUTSEL    | [4:0] |       |      | <b>MIX_OUTSEL</b><br>: Select the audio output for analog mixing out.<br><br>00 : Channel 1                      0E : Channel 15<br>01 : Channel 2                      0F : Channel 16<br>02 : Channel 3                      10 : playback audio<br>03 : Channel 4                      (first stage playback audio)<br>04 : Channel 5                      11 : second playback audio<br>05 : Channel 6                      (middle stage playback audio)<br>06 : Channel 7                      12 : third playback audio<br>07 : Channel 8                      (middle stage playback audio)<br>08 : Channel 9                      13 : fourth playback audio<br>09 : Channel 10                     (last stage playback audio)<br>0A : Channel 11                    14 : Mic input 1<br>0B : Channel 12                    15 : Mic input 2<br>0C : Channel 13                    18 : Mixed audio<br>0D : Channel 14                    Others : No audio output |



● Registers to Select Audio Output for ADATA\_SP PIN

| AD DRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|----------|------|---------------|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank     | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1        | 0x24 | L_CH_OUTSEL   | [4:0] | 0x19  | 0x19 | <b>L_CH_OUTSEL / R_CH_OUTSEL</b><br>: Select Left/Right channel of the audio output for ADATA_SP pin<br><br>00 : Channel 1                      0E : Channel 15<br>01 : Channel 2                      0F : Channel 16<br>02 : Channel 3                      10 : playback audio<br>(first stage playback audio)<br>03 : Channel 4                      11 : second playback audio<br>(middle stage playback audio)<br>04 : Channel 5                      12 : third playback audio<br>(middle stage playback audio)<br>05 : Channel 6                      13 : fourth playback audio<br>(last stage playback audio)<br>06 : Channel 7<br>07 : Channel 8<br>08 : Channel 9<br>09 : Channel 10<br>0A : Channel 11                      14 : Mic input 1<br>0B : Channel 12                      15 : Mic input 2<br>0C : Channel 13                      18 : Mixed audio<br>0D : Channel 14                      Others : No audio output |
|          | 0x25 | R_CH_OUTSEL   |       |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

● Registers to Control Audio Detection

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                            |
|---------|------|---------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                        |
| 1       | 0x26 | MIX_MUTE_01   | [0]  | 0x00  | 0x00 | <b>MIX_MUTE_x</b><br>: During mixing, selected channels are muted ( x = channel value )<br><br>0 : mixing data output<br>1 : mute for selected channel |
|         |      | MIX_MUTE_02   | [1]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_03   | [2]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_04   | [3]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_05   | [4]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_06   | [5]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_07   | [6]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_08   | [7]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_09   | [0]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_10   | [1]  |       |      |                                                                                                                                                        |
|         | 0x27 | MIX_MUTE_11   | [2]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_12   | [3]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_13   | [4]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_14   | [5]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_15   | [6]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_16   | [7]  |       |      |                                                                                                                                                        |
|         | 0x28 | MIX_MUTE_P1   | [0]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_P2   | [1]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_P3   | [2]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_P4   | [3]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_M1   | [4]  |       |      |                                                                                                                                                        |
|         |      | MIX_MUTE_M2   | [5]  |       |      |                                                                                                                                                        |

● Registers to Control Audio Detection

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                  |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                              |
| 1       | 0x29 | AUTO_MUTE     | [7]   | 0x88  | 0x88 | <b>AUTO MUTE Detection</b><br>0 : Don't use this function      1 : Use this function<br>0 : Absolute amplitude detection mode<br>1 : Differential amplitude detection mode                                                                                                                   |
|         |      | ADET_FILT     | [2:0] |       |      | <b>ADET_FILT</b><br>: Set the time to decide the existence of audio signals.<br>0 : 16sec                              1 : 15sec<br>2 : 9sec                                3 : 5sec<br>4 : 3sec                                5 : 1sec<br>6 : 0.6sec                            7 : 0.5sec |

● Registers to Control Audio Detection

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                    |
|---------|------|---------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                |
| 1       | 0x2A | ADET_01       | [0]  | 0xFF  | 0xFF | <b>ADET_0x / ADET_Mx</b><br>: Enable bit audio signal existence checking function for AIN1-4 and MICIN1.<br>(x = channel 1~4 ) |
|         |      | ADET_02       | [1]  |       |      |                                                                                                                                |
|         |      | ADET_03       | [2]  |       |      |                                                                                                                                |
|         |      | ADET_04       | [3]  |       |      |                                                                                                                                |
|         | 0x2B | ADET_M1       | [6]  | 0x40  | 0x40 |                                                                                                                                |

● Registers to Control Audio CLK

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                  |
|---------|------|---------------|------|-------|------|------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                              |
| 1       | 0x38 | AUD_SW_RST    | [4]  | 0x08  | 0x08 | <b>AUD_SW_RST</b><br>: Software Reset<br>0 : Normal Operation      1 : Reset |

● Registers to Control Audio DAC GAIN

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1       | 0x3A | A_DAC_GAIN    | [3:0] | 0x03  | 0x03 | <b>A_DAC_GAIN</b><br>: Digital Input to Analog Output Gain Control<br>Analog output is 2Vpp when gain setting is 0dB and digital input is full scale<br>0 : -3dB                              8 : 5dB<br>1 : -2dB                              9 : 6dB<br>2 : -1dB                              10 : 7dB<br>3 : 0dB                                11 : 8dB<br>4 : 1dB                                12 : 9dB<br>5 : 2dB                                13 : 10dB<br>6 : 3dB                                14 : 11dB<br>7 : 4dB                                15 : 12dB |

● Registers to Control Audio AFE

| ADDRESS |      | REGISTER NAME   | BITS  | VALUE |     | DESCRIPTION                                                          |       |       |      |      |           |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|---------|------|-----------------|-------|-------|-----|----------------------------------------------------------------------|-------|-------|------|------|-----------|------|-------|-------|------|------|------|------|-------|------|------|------|------|------|-------|------|------|------|------|------|-------|------|------|------|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|------|------|------|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|------|------|------|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|--|------|--|------|------|-------|------|------|------|------|
| Bank    | Addr |                 |       | 30P   | 25P |                                                                      |       |       |      |      |           |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
| 1       | 0x3B | A_GAIN_SEL(AFE) | [7:4] | 0x3   | 0x3 | A_GAIN_SEL(AUDIO AFE)<br>: Analog Gain Control for AIN 1 ~ 4, MicIN1 |       |       |      |      |           |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | A_GAIN_SEL<3:0>                                                      | Gain  | Low   | Mid  | High | Input Vpp | 0000 | 0.25x | -0.60 | 1.60 | 3.60 | 4.00 | 0001 | 0.50x | 0.60 | 1.60 | 2.60 | 2.00 | 0010 | 0.75x | 0.93 | 1.60 | 2.27 | 1.33 | 0011 | 1.00x | 1.10 | 1.60 | 2.10 | 1.00 | 0100 | 1.25x |  | 1.60 |  | 0.80 | 0101 | 1.50x |  | 1.60 |  | 0.67 | 0110 | 1.75x |  | 1.60 |  | 0.57 | 0111 | 2.00x | 1.35 | 1.60 | 1.85 | 0.50 | 1000 | 2.25x |  | 1.60 |  | 0.44 | 1001 | 2.50x |  | 1.60 |  | 0.40 | 1010 | 2.75x |  | 1.60 |  | 0.36 | 1011 | 3.00x | 1.54 | 1.60 | 1.77 | 0.33 | 1100 | 3.25x |  | 1.60 |  | 0.31 | 1101 | 3.50x |  | 1.60 |  | 0.29 | 1110 | 3.75x |  | 1.60 |  | 0.27 | 1111 | 4.00x | 1.48 | 1.60 | 1.73 | 0.25 |
|         |      |                 |       |       |     | A_GAIN_SEL<3:0>                                                      | Gain  | Low   | Mid  | High | Input Vpp |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0000                                                                 | 0.25x | -0.60 | 1.60 | 3.60 | 4.00      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0001                                                                 | 0.50x | 0.60  | 1.60 | 2.60 | 2.00      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0010                                                                 | 0.75x | 0.93  | 1.60 | 2.27 | 1.33      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0011                                                                 | 1.00x | 1.10  | 1.60 | 2.10 | 1.00      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0100                                                                 | 1.25x |       | 1.60 |      | 0.80      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0101                                                                 | 1.50x |       | 1.60 |      | 0.67      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0110                                                                 | 1.75x |       | 1.60 |      | 0.57      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 0111                                                                 | 2.00x | 1.35  | 1.60 | 1.85 | 0.50      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1000                                                                 | 2.25x |       | 1.60 |      | 0.44      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1001                                                                 | 2.50x |       | 1.60 |      | 0.40      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1010                                                                 | 2.75x |       | 1.60 |      | 0.36      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1011                                                                 | 3.00x | 1.54  | 1.60 | 1.77 | 0.33      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1100                                                                 | 3.25x |       | 1.60 |      | 0.31      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1101                                                                 | 3.50x |       | 1.60 |      | 0.29      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1110                                                                 | 3.75x |       | 1.60 |      | 0.27      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |
|         |      |                 |       |       |     | 1111                                                                 | 4.00x | 1.48  | 1.60 | 1.73 | 0.25      |      |       |       |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |  |      |  |      |      |       |      |      |      |      |

## 6.2.5 Power Down Registers

### ● Registers to Control Each Channel Reset

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                        |
|---------|------|---------------|------|-------|------|--------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                    |
| 1       | 0x97 | CH_RST_4      | [3]  | 0xF   | 0x0F | <b>CH_RST_x</b><br>: Each Video Channel Reset<br>( x = channel number )<br>0 : Channel_x Reset<br>1 : Channel_x On |
|         |      | CH_RST_3      | [2]  |       |      |                                                                                                                    |
|         |      | CH_RST_2      | [1]  |       |      |                                                                                                                    |
|         |      | CH_RST_1      | [0]  |       |      |                                                                                                                    |

### ● Registers to Control CLK Power Down

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                               |
|---------|------|---------------|------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                           |
| 1       | 0x98 | PD_DEC_4      | [3]  | 0x00  | 0x00 | <b>PD_DEC_x</b><br>: Each Decoder Clock Power Down<br>( x = channel number )<br>0 : Decoder Clock Power On<br>1 : Decoder Clock Power Off |
|         |      | PD_DEC_3      | [2]  |       |      |                                                                                                                                           |
|         |      | PD_DEC_2      | [1]  |       |      |                                                                                                                                           |
|         |      | PD_DEC_1      | [0]  |       |      |                                                                                                                                           |
|         | 0x9A | AUD_RST       | [4]  | 0x0   | 0x0  | <b>AUD_RST</b><br>: Audio Reset<br>0 : Audio On<br>1 : Audio Reset                                                                        |
|         |      | PD_AUD        | [0]  | 0x00  | 0x00 | <b>PD_AUD</b><br>: Audio Clock Power Down                                                                                                 |

## 6.2.6 MPP Control Registers

### ● Registers to Control MPP

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                       |
|---------|------|---------------|------|-------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                                                                                                   |
| 1       | 0xB1 | MPP1_DIR      | [0]  | 0x00  | 0x00 | <b>MPPx_DIR</b><br>: MPPx pin direction control (x = MPP pin number)<br><br>0 : Output Direction<br>1 : Input Direction                                           |
|         |      | MPP2_DIR      | [1]  |       |      |                                                                                                                                                                   |
|         |      | MPP3_DIR      | [2]  |       |      |                                                                                                                                                                   |
|         |      | MPP4_DIR      | [3]  |       |      |                                                                                                                                                                   |
|         | 0xB2 | MPP1_CLK      | [0]  | 0x00  | 0x00 | <b>MPPx_CLK</b><br>: MPPx Clock Enable (x = MPP pin number)<br><br>0 : MPP Signal out from MPPx_pin.<br>1 : Selected Clock among BANK1, 0xB4~BB Out from MPPx_pin |
|         |      | MPP2_CLK      | [1]  |       |      |                                                                                                                                                                   |
|         |      | MPP3_CLK      | [2]  |       |      |                                                                                                                                                                   |
|         |      | MPP4_CLK      | [7]  |       |      |                                                                                                                                                                   |
|         | 0xB3 | MPP1_INV      | [0]  | 0x00  | 0x00 | <b>MPPx_INV</b><br>: MPPx pin output signal inversion (x = MPP pin number)                                                                                        |
|         |      | MPP2_INV      | [1]  |       |      |                                                                                                                                                                   |
|         |      | MPP3_INV      | [2]  |       |      |                                                                                                                                                                   |
|         |      | MPP4_INV      | [3]  |       |      |                                                                                                                                                                   |

### ● Registers to Control MPP

| ADDRESS |      | REGISTER NAME    | BITS  | VALUE |      | DESCRIPTION                                                                                        |
|---------|------|------------------|-------|-------|------|----------------------------------------------------------------------------------------------------|
| Bank    | Addr |                  |       | 30P   | 25P  |                                                                                                    |
| 1       | 0xB4 | MPP_CLK1_SEL     | [7:4] | 0x40  | 0x40 | MPP_CLKx_SEL (x = MPP Pin number)<br>: The Same as VCLKx Condition<br>( VCLK = Bank1 0xCD/CE )     |
|         | 0xB5 | MPP_CLK2_SEL     |       |       |      |                                                                                                    |
|         | 0xB6 | MPP_CLK3_SEL     |       |       |      |                                                                                                    |
|         | 0xB7 | MPP_CLK4_SEL     |       |       |      |                                                                                                    |
|         | 0xB4 | MPP_CLK1_DLY_SEL | [3:0] |       |      | MPP_CLKx_DLY_SEL (x = MPP Pin number)<br>: The Same as VCLKx Condition<br>( VCLK = Bank1 0xCD/CE ) |
|         | 0xB5 | MPP_CLK2_DLY_SEL |       |       |      |                                                                                                    |
|         | 0xB6 | MPP_CLK3_DLY_SEL |       |       |      |                                                                                                    |
|         | 0xB7 | MPP_CLK4_DLY_SEL |       |       |      |                                                                                                    |

## ● Registers to Select Video Output

| ADDRESS |      | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|---------|------|---------------|-------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |               |       | 30P   | 25P  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 1       | 0xC2 | VPORT1_SEQ1   | [3:0] | 0x00  | 0x00 | <b>VPORTx_SEQy</b><br>: Select the type of output video signal through each video output port<br>(x = VDO output port number, y= channel count for 1 port)<br><br>0 : Nomal Display of Channel 1<br>1 : Nomal Display of Channel 2<br>2 : Nomal Display of Channel 3<br>3 : Nomal Display of Channel 4<br>4 : Only Y Display of Channel 1<br>5 : Only Y Display of Channel 2<br>6 : Only Y Display of Channel 3<br>7 : Only Y Display of Channel 4<br>8 : H_CIF Display of Channel 1<br>9 : H_CIF Display of Channel 2<br>A : H_CIF Display of Channel 3<br>B : H_CIF Display of Channel 4<br>C : Only C Display of Channel 1<br>D : Only C Display of Channel 2<br>E : Only C Display of Channel 3<br>F : Only C Display of Channel 4<br><br><b>Etc.:</b> Don't use |
|         |      | VPORT1_SEQ2   | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         | 0xC3 | VPORT1_SEQ3   | [3:0] | 0x00  | 0x00 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         |      | VPORT1_SEQ4   | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         | 0xC4 | VPORT2_SEQ1   | [3:0] | 0x11  | 0x11 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         |      | VPORT2_SEQ2   | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         | 0xC5 | VPORT2_SEQ3   | [3:0] | 0x11  | 0x11 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|         |      | VPORT2_SEQ4   | [7:4] |       |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

- **Registers to Select Video Output**

| ADDRESS |      | REGISTER NAME      | BITS  | VALUE |     | DESCRIPTION                                                                                                                                              |
|---------|------|--------------------|-------|-------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                    |       | 30P   | 25P |                                                                                                                                                          |
| 1       | 0xC8 | VPORT_1_CH_OUT_SEL | [7:4] | 0x2   | 0x2 | <b>VPORT_x_CH_OUT_SEL</b><br>: Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) |
|         | 0xC9 | VPORT_2_CH_OUT_SEL | [3:0] | 0x2   | 0x2 | <b>0</b> : 1-Port 1CH data<br><b>2</b> : 1-Port 2CH time-mixed data<br><b>8</b> : 1-Port 4CH time-mixed data<br><b>Etc.:</b> Don't use                   |

- **Registers to Control Video Output Port Enable**

| ADDRESS |      | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                       |
|---------|------|---------------|------|-------|------|-----------------------------------------------------------------------------------|
| Bank    | Addr |               |      | 30P   | 25P  |                                                                                   |
| 1       | 0xCA | VCLK_2_EN     | [6]  | 0x66  | 0x66 | <b>VCLK_x_EN</b><br>: Video Output Port_x CLK Enable (x = VDO output port number) |
|         |      | VCLK_1_EN     | [5]  |       |      | 0 : Disable <span style="float: right;">1 : Enable</span>                         |
|         |      | VDO_2_EN      | [2]  |       |      | <b>VDO_x_EN</b><br>: VDOx Port Enable (x = VDO output port number)                |
|         |      | VDO_1_EN      | [1]  |       |      | 0 : Disable <span style="float: right;">1 : Enable</span>                         |

● Registers to Control Data

| ADDRESS |      | REGISTER NAME  | BITS | VALUE |      | DESCRIPTION                                                                                        |
|---------|------|----------------|------|-------|------|----------------------------------------------------------------------------------------------------|
| Bank    | Addr |                |      | 30P   | 25P  |                                                                                                    |
| 1       | 0xCB | OUT_DATA_2_INV | [2]  | 0x00  | 0x00 | OUT_DATA_x_INV<br>: It sorts output video data inversely.<br>(0 : [7:0], 1 : [0:7])                |
|         |      | OUT_DATA_1_INV | [1]  |       |      | OUT_DATA_1_INV : VDO1 Port output order control<br>OUT_DATA_2_INV : VDO2 Port output order control |

● Registers to Select Video Output Clock

| ADDRESS |      | REGISTER NAME        | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                                                                                                                              |
|---------|------|----------------------|-------|-------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                      |       | 30P   | 25P  |                                                                                                                                                                                                                                                                          |
| 1       | 0xCD | VPORT_1_OCLK_SEL     | [7:4] | 0x46  | 0x46 | <b>VPORT_x_OVCLK_SEL</b><br>: Select clock frequency and phase of each port. (x = Port number)<br><br>0~3 : PLL divided by 4 with phase#1~4 (74.25Mhz)<br>4~5 : PLL divided by 2 with phase#1~2 (148.5Mhz)<br>8~B : PLL divided by 8 with phase#1~4(37.125Mhz)           |
|         | 0xCE | VPORT_2_OCLK_SEL     |       |       |      |                                                                                                                                                                                                                                                                          |
|         | 0xCD | VPORT_1_OCLK_DLY_SEL | [3:0] |       |      | <b>VPORT_x_OVCLK_DLY_SEL</b><br>: Delay the output clock in the unit of $\approx (VCLK / 16)$ ns. Can be delayed up (x = Port number)<br><br>0 : $\approx (VCLK / 16) * 0$ ns.<br>4 : $\approx (VCLK / 16) * 4$ ns<br><br># Delay value = (VCLK / 16) * DLY_SEL Value ns |
|         | 0xCE | VPORT_2_OCLK_DLY_SEL |       |       |      |                                                                                                                                                                                                                                                                          |

## 6.2.8 MOTION Registers

### ● Registers to Detect Motion

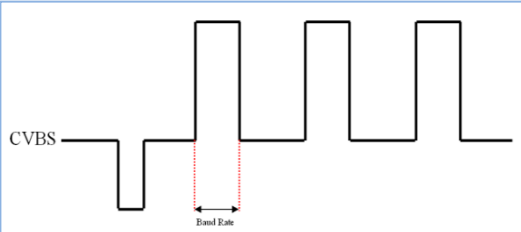
| ADDRESS |      | REGISTER NAME  | BITS | VALUE |      | DESCRIPTION                                                                                                                                        |
|---------|------|----------------|------|-------|------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr |                |      | FHD   | HD   |                                                                                                                                                    |
| 2       | 0x00 | CH1_MOTION_OFF | [0]  | 0xED  | 0x09 | <b>CHx_MOTION_OFF</b><br>: Motion Detection On/Off Selection ( x = channel number )<br><br>0 : Motion detection on<br><br>1 : Motion detection off |
|         | 0x07 | CH2_MOTION_OFF |      |       |      |                                                                                                                                                    |
|         | 0x0E | CH3_MOTION_OFF |      |       |      |                                                                                                                                                    |
|         | 0x15 | CH4_MOTION_OFF |      |       |      |                                                                                                                                                    |



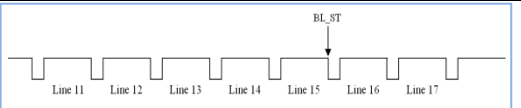
## 6.2.9 COAXIAL Registers

- CH1 Coaxial Register : Bank3 0x00~0x7F
- CH2 Coaxial Register : Bank3 0x80~0xFF
- CH3 Coaxial Register : Bank4 0x00~0x7F
- CH4 Coaxial Register : Bank4 0x80~0xFF

### ● Registers to Control Baud Rate

| ADDRESS                  |             | REGISTER NAME  | BITS  | VALUE |      | DESCRIPTION                                                                        |
|--------------------------|-------------|----------------|-------|-------|------|------------------------------------------------------------------------------------|
| Bank                     | Addr        |                |       | 30P   | 25P  |                                                                                    |
| 3~4                      | 0x00 / 0x80 | CHx_BAUD       | [7:0] | 0x27  | 0x27 | CHx_BAUD (x = Channel Number)<br>: A-CP TX Baud Rate                               |
|                          | 0x02 / 0x82 | CHx_PELCO_BAUD | [7:0] | 0x1B  | 0x1B | CHx_PELCO_BAUD (x = Channel Number)<br>: PELCO TX Baud Rate                        |
| Coaxial protocol 1H Line |             |                |       |       |      |  |

### ● Registers to Control Start Point of VBI(Vertical Blank Interval)

| ADDRESS                                                             |             | REGISTER NAME         | BITS  | VALUE |      | DESCRIPTION                                                                          |
|---------------------------------------------------------------------|-------------|-----------------------|-------|-------|------|--------------------------------------------------------------------------------------|
| Bank                                                                | Addr        |                       |       | 30P   | 25P  |                                                                                      |
| 3~4                                                                 | 0x04 / 0x84 | CHx_BL_TXST[15:8]     | [7:0] | 0x00  | 0x00 | CHx_BL_TXST (x = Channel Number)<br>: A-CP Protocol TX start Line in VBI             |
|                                                                     | 0x03 / 0x83 | CHx_BL_TXST[7:0]      | [7:0] | 0x0E  | 0x0E |                                                                                      |
|                                                                     | 0x05 / 0x85 | CHx_ACT_LEN           | [3:0] | 0x03  | 0x03 | CHx_ACT_LEN (x = Channel Number)<br>: A-CP Line number                               |
|                                                                     | 0x08 / 0x88 | CHx_PELCO_TXST [15:8] | [7:0] | 0x00  | 0x00 | CHx_PELCO_TXST (x = Channel Number)<br>: PELCO Protocol TX Start Line in VBI         |
|                                                                     | 0x07 / 0x87 | CHx_PELCO_TXST [7:0]  | [7:0] | 0x0E  | 0x0E |                                                                                      |
| Coaxial protocol Active Start Point of VBI(Vertical Blank Interval) |             |                       |       |       |      |  |

● Registers to Control Coaxial Protocol

| ADDRESS |                   | REGISTER NAME      | BITS  | VALUE |      | DESCRIPTION                                                                                                                                                           |
|---------|-------------------|--------------------|-------|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr              |                    |       | 30P   | 25P  |                                                                                                                                                                       |
| 3~4     | 0x09<br>/<br>0x89 | CHx_COAX_SW_RST    | [4]   | 0x08  | 0x08 | CHx_COAX_SW_RST (x = Channel Number)<br>: Coaxial Software Reset                                                                                                      |
|         |                   | CHx_CNT_MODE       | [3]   |       |      | CHx_CNT_MODE (x = Channel Number)<br>: A-CP Protocol Enable Signal                                                                                                    |
|         |                   | CHx_TX_START       | [0]   |       |      | CHx_TX_START (x = Channel Number)<br>: A-CP Protocol Enable Signal                                                                                                    |
|         | 0x0A<br>/<br>0x8A | CHx_TX_BYTE_LENGTH | [4:0] | 0x03  | 0x03 | CHx_TX_BYTE_LENGTH (x = Channel Number)<br>: Transmission amount in A-CP Protocol                                                                                     |
|         | 0x0B<br>/<br>0x8B | CHx_PELCO_8BIT     | [7]   | 0x10  | 0x10 | CHx_PELCO_8BIT (x = Channel Number)<br>: Pelco Protocol 8Bit mode Selection<br>0 : Pelco Protocol Exp mode<br>1 : Pelco Protocol 8bit mode                            |
|         |                   | CHx_LINE_8BIT      | [4]   |       |      | CHx_LINE_8BIT (x = Channel Number)<br>: A-CP Protocol Origin Mode Selection<br>0 : Pelco Protocol Mode<br>1 : A-CP Protocol Origin Mode                               |
|         |                   | CHx_PACKET_MODE    | [2:0] |       |      | CHx_PACKET_MODE (x = Channel Number)<br>: Coaxial Protocol Type<br>2 : Pelco Protocol Origin Mode<br>4 : Pelco Protocol Exp mode(Pelco_32bit Mode)<br>Others : Manual |
|         | 0x0C<br>/<br>0x8C | CHx_PELCO_CTEN     | [0]   | 0x00  | 0x00 | CHx_PELCO_CTEN (x = Channel Number)<br>: PELCO Protocol Enable Bit (Active High)                                                                                      |
|         | 0x0E<br>/<br>0x8E | CHx_BL_HSP [15:7]  | [7:0] | 0x00  | 0x02 | CHx_BL_HSP (x = Channel Number)<br>: Start Point in Coaxial Protocol Active Line                                                                                      |
|         | 0x0D<br>/<br>0x8D | CHx_BL_HSP [7:0]   | [7:0] | 0xB4  | 0x48 |                                                                                                                                                                       |
|         | 0x0F<br>/<br>0x8F | CHx_PELCO_SHOT     | [0]   | 0x00  | 0x00 | CHx_PELCO_SHOT (x = Channel Number)<br>: PELCO Protocol One Operation Enable signal                                                                                   |

● Registers to Control Coaxial Data

| ADDRESS |                   | REGISTER NAME  | BITS  | VALUE |      | DESCRIPTION                                                                                           |
|---------|-------------------|----------------|-------|-------|------|-------------------------------------------------------------------------------------------------------|
| Bank    | Addr              |                |       | 30P   | 25P  |                                                                                                       |
| 3~4     | 0x10<br>/<br>0x90 | CHx_TX_DATA_01 | [7:0] | 0x00  | 0x00 | CHx_TX_DATA_01 ~ CHx_TX_DATA_04 (x = Channel Number)<br>: 1 <sup>st</sup> field Data in A-CP Protocol |
|         | 0x11<br>/<br>0x91 | CHX_TX_DATA_02 | [7:0] | 0x10  | 0x10 |                                                                                                       |
|         | 0x12<br>/<br>0x92 | CHX_TX_DATA_03 | [7:0] | 0x18  | 0x18 |                                                                                                       |
|         | 0x13<br>/<br>0x93 | CHX_TX_DATA_04 | [7:0] | 0xFF  | 0xFF |                                                                                                       |
|         | 0x14<br>/<br>0x94 | CHX_TX_DATA_05 | [7:0] | 0xAA  | 0xAA | CHx_TX_DATA_05 ~ CHx_TX_DATA_08 (x = Channel Number)<br>: 2 <sup>nd</sup> field Data in A-CP Protocol |
|         | 0x15<br>/<br>0x95 | CHX_TX_DATA_06 | [7:0] | 0x3C  | 0x3C |                                                                                                       |
|         | 0x16<br>/<br>0x96 | CHX_TX_DATA_07 | [7:0] | 0xFF  | 0xFF |                                                                                                       |
|         | 0x17<br>/<br>0x97 | CHX_TX_DATA_08 | [7:0] | 0xFF  | 0xFF |                                                                                                       |
|         | 0x18<br>/<br>0x98 | CHX_TX_DATA_09 | [7:0] | 0xAA  | 0xAA | CHx_TX_DATA_09 ~ CHx_TX_DATA_12 (x = Channel Number)<br>: 3 <sup>rd</sup> field Data in A-CP Protocol |
|         | 0x19<br>/<br>0x99 | CHX_TX_DATA_10 | [7:0] | 0x1B  | 0x1B |                                                                                                       |
|         | 0x1A<br>/<br>0x9A | CHX_TX_DATA_11 | [7:0] | 0x00  | 0x00 |                                                                                                       |
|         | 0x1B<br>/<br>0x9B | CHX_TX_DATA_12 | [7:0] | 0x00  | 0x00 |                                                                                                       |
|         | 0x1C<br>/<br>0x9C | CHX_TX_DATA_13 | [7:0] | 0xAA  | 0xAA | CHx_TX_DATA_13 ~ CHx_TX_DATA_16 (x = Channel Number)<br>: 4 <sup>th</sup> field Data in A-CP Protocol |
|         | 0x1D<br>/<br>0x9D | CHX_TX_DATA_14 | [7:0] | 0x3B  | 0x3B |                                                                                                       |
|         | 0x1E<br>/<br>0x9E | CHX_TX_DATA_15 | [7:0] | 0x00  | 0x00 |                                                                                                       |
|         | 0x1F<br>/<br>0x9F | CHX_TX_DATA_16 | [7:0] | 0x00  | 0x00 |                                                                                                       |

● Registers to Control Coaxial Data

| ADDRESS |                   | REGISTER NAME      | BITS  | VALUE |      | DESCRIPTION                                                                                                      |
|---------|-------------------|--------------------|-------|-------|------|------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr              |                    |       | 30P   | 25P  |                                                                                                                  |
| 3~4     | 0x20<br>/<br>0xA0 | CHx_PELCO_TXDAT_01 | [7:0] | 0x00  | 0x00 | CHx_PELCO_TXDAT_01 ~ CHx_PELCO_TXDAT_02<br>: 18 <sup>th</sup> Line in PELCO Protocol<br><br>(x = Channel Number) |
|         | 0x21<br>/<br>0xA1 | CHx_PELCO_TXDAT_02 | [7:0] | 0x00  | 0x00 |                                                                                                                  |
|         | 0x22<br>/<br>0xA2 | CHx_PELCO_TXDAT_03 | [7:0] | 0x00  | 0x00 | CHx_PELCO_TXDAT_03 ~ CHx_PELCO_TXDAT_04<br>: 19 <sup>th</sup> Line in PELCO Protocol<br><br>(x = Channel Number) |
|         | 0x23<br>/<br>0xA3 | CHx_PELCO_TXDAT_04 | [7:0] | 0x00  | 0x00 |                                                                                                                  |

● Registers to Control Coaxial Protocol

| ADDRESS |             | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                  |
|---------|-------------|---------------|-------|-------|------|------------------------------------------------------------------------------|
| Bank    | Addr        |               |       | 30P   | 25P  |                                                                              |
| 3~4     | 0x2C / 0xAC | CHx_VSO_INV   | [7:0] | 0x00  | 0x00 | CHx_VSO_INV (x = Channel Number)<br>: Vertical Sync Inverter (Active High)   |
|         | 0x2D / 0xAD | CHx_HSO_INV   | [7:0] | 0x00  | 0x00 | CHx_HSO_INV (x = Channel Number)<br>: Horizontal Sync Inverter (Active High) |
|         | 0x2F / 0xAF | CHx_EVEN_SUM  | [7:0] | 0x00  | 0x00 | Control Protocol Active line on each field                                   |

● Registers to Control Coaxial Protocol

| ADDRESS |             | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                                                                                                                                              |
|---------|-------------|---------------|------|-------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bank    | Addr        |               |      | 30P   | 25P  |                                                                                                                                                                                          |
| 3~4     | 0x3A / 0xBA | CHx_CLEAN     | [0]  | 0x00  | 0x00 | CHx_CLEAN (x = Channel Number)<br>: RX Register is Read Only. So it need clean Condition<br>First, this register set ON. Second, Read I2C Protocol 0x90.<br>And then Clean RX Registers. |

● Registers to Read Coaxial Status

| ADDRESS |             | REGISTER NAME  | BITS  | VALUE |      | DESCRIPTION                                                                                      |
|---------|-------------|----------------|-------|-------|------|--------------------------------------------------------------------------------------------------|
| Bank    | Addr        |                |       | 30P   | 25P  |                                                                                                  |
| 3~4     | 0x50 / 0xD0 | CHx_PELCO_8_00 | [7:0] | Read  | Read | CHx_PELCO_8_00 ~ CHx_PELCO_8_07 (x = Channel Number)<br>: Coaxial Output 8bit Data Read Register |
|         | 0x51 / 0xD1 | CHx_PELCO_8_01 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x52 / 0xD2 | CHx_PELCO_8_02 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x53 / 0xD3 | CHx_PELCO_8_03 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x54 / 0xD4 | CHx_PELCO_8_04 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x55 / 0xD5 | CHx_PELCO_8_05 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x56 / 0xD6 | CHx_PELCO_8_06 | [7:0] | Read  | Read |                                                                                                  |
|         | 0x57 / 0xD7 | CHx_PELCO_8_07 | [7:0] | Read  | Read |                                                                                                  |

● Registers to Read Coaxial Status

| ADDRESS |             | REGISTER NAME | BITS | VALUE |      | DESCRIPTION                                                   |
|---------|-------------|---------------|------|-------|------|---------------------------------------------------------------|
| Bank    | Addr        |               |      | 30P   | 25P  |                                                               |
| 3~4     | 0x5C / 0xDC | CHx_RX_DONE   | [0]  | Read  | Read | CHx_RX_DONE (x = Channel Number)<br>: Coaxial RX Request Done |

● Registers to Read Coaxial Status

| ADDRESS |             | REGISTER NAME    | BITS  | VALUE |      | DESCRIPTION                                                          |
|---------|-------------|------------------|-------|-------|------|----------------------------------------------------------------------|
| Bank    | Addr        |                  |       | 30P   | 25P  |                                                                      |
| 3~4     | 0x5D / 0xDD | CHx_RX_COAX_DUTY | [7:0] | Read  | Read | CHx_RX_COAX_DUTY (x = Channel Number)<br>: Coaxial RX 8bit DUTY Read |

● Registers to Control Coaxial Protocol

| ADDRESS |                | REGISTER NAME | BITS  | VALUE |      | DESCRIPTION                                                                     |
|---------|----------------|---------------|-------|-------|------|---------------------------------------------------------------------------------|
| Bank    | Addr           |               |       | 30P   | 25P  |                                                                                 |
| 3~4     | 0x60<br>/ 0xE0 | CHx_DEVICE_ID | [7:0] | 0x84  | 0x84 | CHx_DEVICE_ID (x = Channel Number)<br>: Define Device_ID in Protocol's Header   |
|         | 0x62<br>/ 0xE2 | CHx_RX_AREA   | [7:0] | 0x06  | 0x06 | CHx_RX_AREA (x = Channel Number)<br>: Coaxial RX Area 8-bit                     |
|         | 0x63<br>/ 0xE3 | CHx_DELAY_ON  | [4]   | 0x01  | 0x01 | CHx_DELAY_ON (x = Channel Number)<br>: Enable to use DELAY CNT Register         |
|         |                | CHx_COMM_ON   | [0]   |       |      | CHx_COMM_ON (x = Channel Number)<br>: Coaxial RX Software Reset                 |
|         | 0x64<br>/ 0xE4 | CHx_DELAY_CNT | [7:0] | 0x00  | 0x00 | CHx_DELAY_CNT (x = Channel Number)<br>: How many delay input signal based clock |

● Registers to Control Coaxial Protocol

| ADDRESS |                | REGISTER NAME         | BITS  | VALUE |      | DESCRIPTION                                                                    |
|---------|----------------|-----------------------|-------|-------|------|--------------------------------------------------------------------------------|
| Bank    | Addr           |                       |       | 30P   | 25P  |                                                                                |
| 3~4     | 0x65<br>/ 0xE5 | CHx_MSB               | [0]   | 0x01  | 0x01 | CHx_MSB (x = Channel Number)<br>: Coaxial RX MSB Change Mode                   |
|         | 0x66<br>/ 0xE6 | CHx_A_DUTY_ON         | [7]   | 0x80  | 0x80 | CHx_A_DUTY_ON (x = Channel Number)<br>: Coaxial RX DUTY Mode                   |
|         | 0x67<br>/ 0xE7 | CHx_INT_MODE          | [0]   | 0x01  | 0x01 | CHx_INT_MODE (x = Channel Number)<br>: Coaxial RX Interrupt Mode               |
|         | 0x68<br>/ 0xE8 | CHx_RX_SZ             | [7:4] | 0x50  | 0x50 | CHx_RX_SZ (x = Channel Number)<br>: Coaxial RX Line MAX Set                    |
|         | 0x69<br>/ 0xE9 | CH1_M_DUTY            | [7:0] | 0x00  | 0x00 | CH1_M_DUTY (x = Channel Number)<br>: Coaxial RX DUTY Set                       |
|         | 0x6A<br>/ 0xEA | CH1_RX_START_POSITION | [7:0] | 0x00  | 0x00 | CH1_RX_START_POSITION (x = Channel Number)<br>: Coaxial RX Start Point in Line |

● Registers to Read Coaxial Status

| ADDRESS |                | REGISTER NAME         | BITS  | VALUE |      | DESCRIPTION                                                                       |
|---------|----------------|-----------------------|-------|-------|------|-----------------------------------------------------------------------------------|
| Bank    | Addr           |                       |       | 30P   | 25P  |                                                                                   |
| 3~4     | 0x6C<br>/ 0xEC | CHx_PELCO16_00 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_00 (x = Channel Number)<br>: Coaxial Output 16bit Data1 Read Register |
|         | 0x6D<br>/ 0xED | CHx_PELCO16_00 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x6E<br>/ 0xEE | CHx_PELCO16_01 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_01 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x6F<br>/ 0xEF | CHx_PELCO16_01 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x70<br>/ 0xF0 | CHx_PELCO16_02 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_02 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x71<br>/ 0xF1 | CHx_PELCO16_02 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x72<br>/ 0xF2 | CHx_PELCO16_03 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_03 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x73<br>/ 0xF3 | CHx_PELCO16_03 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x74<br>/ 0xF4 | CHx_PELCO16_04 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_04 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x75<br>/ 0xF5 | CHx_PELCO16_04 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x76<br>/ 0xF6 | CHx_PELCO16_05 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_05 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x77<br>/ 0xF7 | CHx_PELCO16_05 [15:8] | [7:0] | Read  | Read |                                                                                   |
|         | 0x78<br>/ 0xF8 | CHx_PELCO16_06 [7:0]  | [7:0] | Read  | Read | CHx_PELCO16_06 (x = Channel Number)<br>: Coaxial Output 16bit Data2 Read Register |
|         | 0x79<br>/ 0xF9 | CHx_PELCO16_06 [15:8] | [7:0] | Read  | Read |                                                                                   |

\* Registers of Bank 5 ~ Bank 10 are not for users.

In this regard, please refer to the Guide note.

# Chapter 7

## Guide Note

### 7.1 Video Format Setting Register

| Mode |          | CH | SP_MD     | SD_MD     | HD_MD     | ADC_CLK   | PRE_CLK   | DEC_CLK   | VCLK         |
|------|----------|----|-----------|-----------|-----------|-----------|-----------|-----------|--------------|
|      |          | 1  | 0x85[3:0] | 0x81[7:4] | 0x81[3:0] | 1x84[3:0] | 1x8C[3:0] | 1x8C[7:4] | A: 1xCD[7:4] |
|      |          | 2  | 0x86[3:0] | 0x82[7:4] | 0x82[3:0] | 1x85[3:0] | 1x8D[3:0] | 1x8D[7:4] | B: 1xCE[7:4] |
|      |          | 3  | 0x87[3:0] | 0x83[7:4] | 0x83[3:0] | 1x86[3:0] | 1x8E[3:0] | 1x8E[7:4] |              |
|      |          | 4  | 0x88[3:0] | 0x84[7:4] | 0x84[3:0] | 1x87[3:0] | 1x8F[3:0] | 1x8F[7:4] |              |
| AHD  | 1080P_30 |    | 0         | 0         | 2         | 0~3       | 0~3       | 4~5       | 4~5          |
|      | 1080P_25 |    | 0         | 0         | 3         | 0~3       | 0~3       | 4~5       | 4~5          |
|      | 720P_60  |    | 0         | 0         | 4         | 0~3       | 0~3       | 4~5       | 4~5          |
|      | 720P_50  |    | 0         | 0         | 5         | 0~3       | 0~3       | 4~5       | 4~5          |
|      | 720P_30  |    | 0         | 0         | A         | 8~B       | 8~B       | 4~5       | 4~5          |
|      | 720P_25  |    | 0         | 0         | B         | 8~B       | 8~B       | 4~5       | 4~5          |
|      | SD_NT    |    | 0         | C         | 0         | 6~7       | 6~7       | 4~5       | 4~5          |
|      | SD_PAL   |    | 0         | D         | 0         | 6~7       | 6~7       | 4~5       | 4~5          |

### 7.2 Each Format FSC Setting Register

| Mode |          | CH | Register BANK9 |      |      |      |
|------|----------|----|----------------|------|------|------|
|      |          | 1  | 0x50           | 0x51 | 0x52 | 0x53 |
|      |          | 2  | 0x54           | 0x55 | 0x56 | 0x57 |
|      |          | 3  | 0x58           | 0x59 | 0x5A | 0x5B |
|      |          | 4  | 0x5C           | 0x5D | 0x5E | 0x5F |
| AHD  | 1080P_30 |    | 0x2C           | 0xF0 | 0xCA | 0x52 |
|      | 1080P_25 |    | 0xAB           | 0x7D | 0xC3 | 0x52 |
|      | 720P_60  |    | 0x2C           | 0xF9 | 0xC5 | 0x52 |
|      | 720P_50  |    | 0x2C           | 0xE7 | 0xCF | 0x52 |
|      | 720P_30  |    | 0xED           | 0x00 | 0xE5 | 0x4E |
|      | 720P_25  |    | 0x45           | 0x08 | 0x10 | 0x4F |
|      | SD_NT    |    | 0x1E           | 0x7C | 0xF0 | 0x21 |
|      | SD_PAL   |    | 0xCB           | 0x8A | 0x09 | 0x2A |

### 7.3 When Auto Detection, Video Format Classifier

| Resolution | Field rate | Read Register value<br>(Bank5~8 0xF0) | MODE        |
|------------|------------|---------------------------------------|-------------|
| SD, 480i   | 60i        | 0x00                                  | SD_480i60   |
| SD, 576i   | 50i        | 0x10                                  | SD_576i50   |
| AHD, 720p  | 30         | 0x20                                  | AHD_720p30  |
|            | 25         | 0x21                                  | AHD_720p25  |
|            | 60         | 0x22                                  | AHD_720p60  |
|            | 50         | 0x23                                  | AHD_720p50  |
| AHD, 1080p | 30         | 0x30                                  | AHD_1080p30 |
|            | 25         | 0x31                                  | AHD_1080p25 |

### 7.4 Coaxial Setting Register

| AHD  |            |                      |       |      |      |      |           |
|------|------------|----------------------|-------|------|------|------|-----------|
| bank | addr       | description          | 1080p |      | 720p |      |           |
|      |            |                      | 30p   | 25p  | 30p  | 25p  | 60p 50p   |
| 5~8  | 0x7C       | COAX_RX_SYNC/SRC SEL | 0x11  |      | 0x11 |      | 0x01      |
| 3~4  | 0x00/ 0x80 | CHx_BAUD             | 0x27  |      | 0x15 |      | 0x1A      |
|      | 0x03/ 0x83 | CHx_BL_TXST          | 0x0E  | 0x0D | 0x0E | 0x0D | 0x0E 0x0D |
|      | 0x0D/ 0x8D | BL_HSP               | 0x48  | 0xB4 | 0x30 | 0x35 | 0x20 0x16 |
|      | 0x0E/ 0x8E | BL_HSP               | 0x02  | 0x00 | 0x00 |      | 0x00      |
|      | 0x05/ 0x85 | CHx_ACT_LEN          | 0x03  |      | 0x03 |      | 0x03      |
|      | 0x0A/ 0x8A | CHx_TX_BYTE_LENGTH   | 0x03  |      | 0x03 |      | 0x03      |
|      | 0x0B/ 0x8B | CHx_PELCO_8BIT       | 0x10  |      | 0x10 |      | 0x10      |
|      | 0x2F/ 0xAF | CHx_EVEN_SUM         | 0x00  |      | 0x00 |      | 0x00      |

※ If you want to know about 3/4/5M NRT format, please contact us(sales@nextchip.com).



# Chapter 8

## ELECTRICAL CHARACTERISTICS

### 8.1 ABSOLUTE MAXIMUM RATINGS

| PARAMETER                      | SYMBOL            | MIN. | TYP. | MAX.          | UNIT | REMARKS |
|--------------------------------|-------------------|------|------|---------------|------|---------|
| 1.2V Power Supply Voltage      | VDD1A/<br>VDD1D   | -0.5 | -    | 1.8           | V    |         |
| 3.3V Power Supply Voltage      | VDD3A/<br>VDD3D   | -0.5 | -    | 4.6           | V    |         |
| Voltage for Digital Input pins | V <sub>DI</sub>   | -0.5 | -    | VDD3D+<br>0.5 | V    |         |
| Voltage for Analog Input pins  | V <sub>AI</sub>   | -0.5 | -    | 1.92          | V    |         |
| Storage Temperature            | T <sub>S</sub>    | -50  | -    | 150           | ℃    |         |
| Junction Temperature           | T <sub>J</sub>    | -40  | -    | 125           | ℃    |         |
| Vapor phase soldering (15 Sec) | T <sub>VSOL</sub> | -    | -    | 220           | ℃    |         |

\* **Note** : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

### 8.2 RECOMMENDED OPERATING CONDITION

| PARAMETER                     | SYMBOL          | MIN. | TYP. | MAX. | UNIT | REMARKS |
|-------------------------------|-----------------|------|------|------|------|---------|
| 1.2V Power Supply Voltage     | VDD1A/<br>VDD1D | 1.1  | 1.2  | 1.3  | V    |         |
| 3.3V Power Supply Voltage     | VDD3A/<br>VDD3D | 3.0  | 3.3  | 3.6  | V    |         |
| Ambient operating temperature | V <sub>A</sub>  | 0    | -    | 70   | ℃    |         |

### 8.3 DC CHARACTERISTICS

| PARAMETER                        | SYMBOL           | MIN. | TYP. | MAX.      | UNIT | REMARKS |
|----------------------------------|------------------|------|------|-----------|------|---------|
| Input Low Voltage                | V <sub>IL</sub>  | -0.3 | -    | 0.8       | V    |         |
| Input High Voltage               | V <sub>IH</sub>  | 2    | -    | VDD3D+0.3 | V    |         |
| Input Leakage Current            | I <sub>L</sub>   | -    | -    | ±10       | uA   |         |
| Input Capacitance                | C <sub>IN</sub>  | -    | 5    | -         | pF   |         |
| Output Low Voltage               | V <sub>OL</sub>  | -    | -    | 0.4       | V    |         |
| Output High Voltage              | V <sub>OH</sub>  | 2.4  | -    | -         | V    |         |
| Tri-State Output Leakage Current | I <sub>OZ</sub>  | -    | -    | ±10       | uA   |         |
| Output Capacitance               | C <sub>OUT</sub> | -    | 5    | -         | pF   |         |

## 8.4 AC CHARACTERISTICS

| PARAMETER                                        | SYMBOL          | MIN. | TYP. | MAX. | UNIT | REMARKS |
|--------------------------------------------------|-----------------|------|------|------|------|---------|
| ( Power Supply Current )                         |                 |      |      |      |      |         |
| 1.2V Digital Power Supply Current                | $I_{VDD1D}$     | -    | TBD  | -    | mA   |         |
| 3.3V Digital Power Supply Current                | $I_{VDD3D}$     | -    | TBD  | -    | mA   |         |
| 1.2V Analog Power Supply Current                 | $I_{VDD1A}$     |      | TBD  |      | mA   |         |
| 3.3V Analog Power Supply Current                 | $I_{VDD3A}$     | -    | TBD  | -    | mA   |         |
| ( Clock Pin )                                    |                 |      |      |      |      |         |
| SYS_CLK frequency                                | $f_{SYS\_CLK}$  | -    | 27.0 | -    | MHz  |         |
| SYS_CLK duty cycle                               | $f_{DUTY}$      | 45   | -    | 55   | %    |         |
| ( Reset Pin )                                    |                 |      |      |      |      |         |
| RSTB setup time                                  | $t_{SU}$        | 1    |      |      | uSec |         |
| RSTB pulse width low                             | $t_{PWL\_rstb}$ | 1    |      |      | uSec |         |
| RSTB release time (low to high)                  | $t_{REL\_rstb}$ | 10   |      |      | uSec |         |
| ( Host Interface Pins )                          |                 |      |      |      |      |         |
| SCL clock frequency                              | $f_{SCL}$       | -    | 100  | 400  | kHz  |         |
| Hold time(repeated) START condition.             | $t_{HD:STA}$    | 0.6  | -    | -    | uSec |         |
| LOW period of the SCL clock                      | $t_{LOW}$       | 1.3  | -    | -    | uSec |         |
| HIGH period of the SCL clock                     | $t_{HIGH}$      | 0.6  | -    | -    | uSec |         |
| Set-up time for a repeated START condition       | $t_{SU:STA}$    | 0.6  | -    | -    | uSec |         |
| Data hold time                                   | $t_{HD\_DAT}$   | 0    | -    | 0.9  | uSec |         |
| Data set-up time                                 | $t_{SU\_DAT}$   | 100  | -    | -    | ns   |         |
| Rise time of both SDA and SCL signals            | $t_r$           | 20   | -    | 300  | ns   |         |
| Fall time of both SDA and SCL signals            | $t_f$           | 20   | -    | 300  | ns   |         |
| Set-up time for STOP condition                   | $t_{SU:STO}$    | 0.6  | -    | -    | uSec |         |
| Bus free time between a STOP and START condition | $t_{BUF}$       | 1.3  | -    | -    | uSec |         |
| Capacitive load for each bus line                | $C_b$           | -    | -    | 400  | pF   |         |

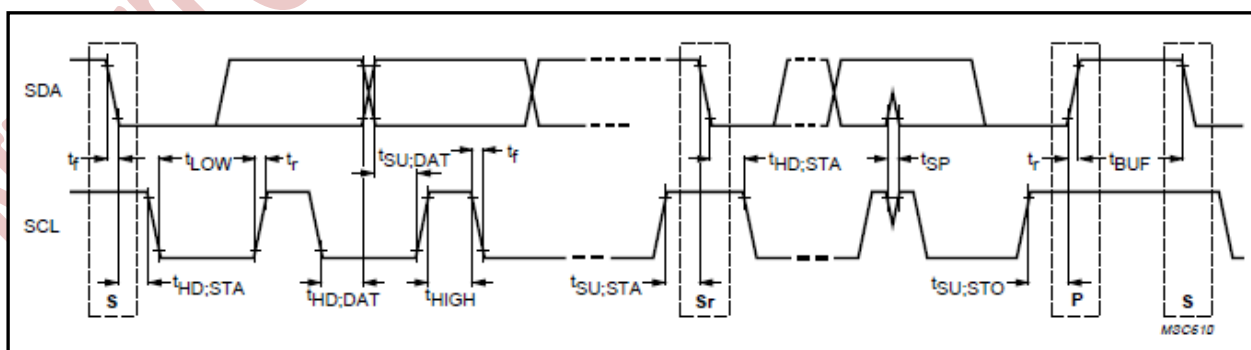


Figure 8.1 SCL and SDA Timing Diagram

# Chapter 9

## AUDIO SYSTEM APPLICATIONS

### 9.1 AUDIO 4-Channel Mode

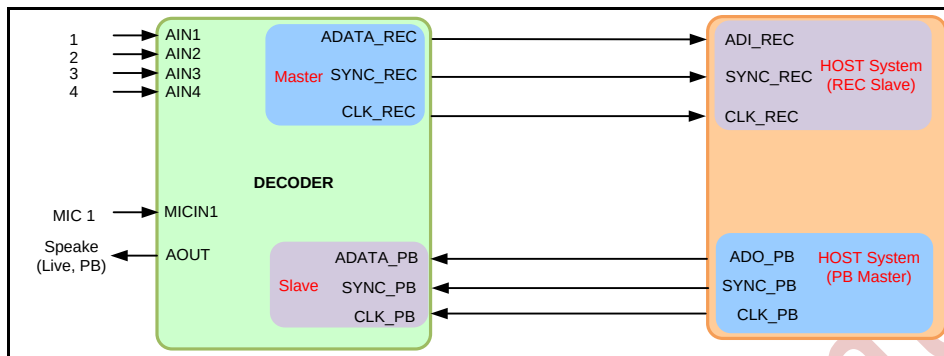


Figure 9.1 AUDIO 4-channel Mode

### 9.2 AUDIO 8-Channel Mode

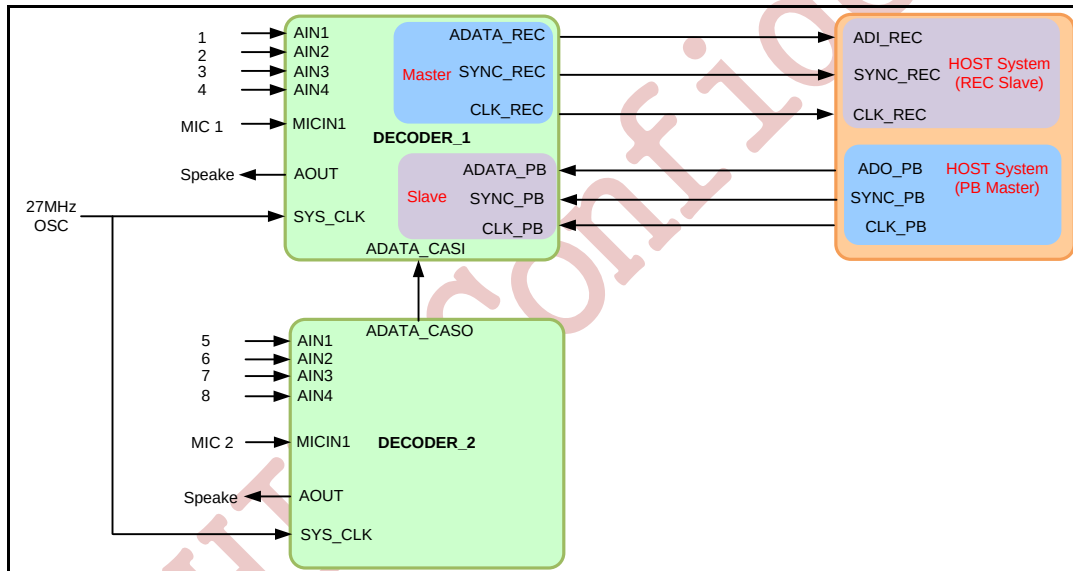


Figure 9.2 AUDIO 8-channel Mode

### 9.3 AUDIO 16-Channel Mode

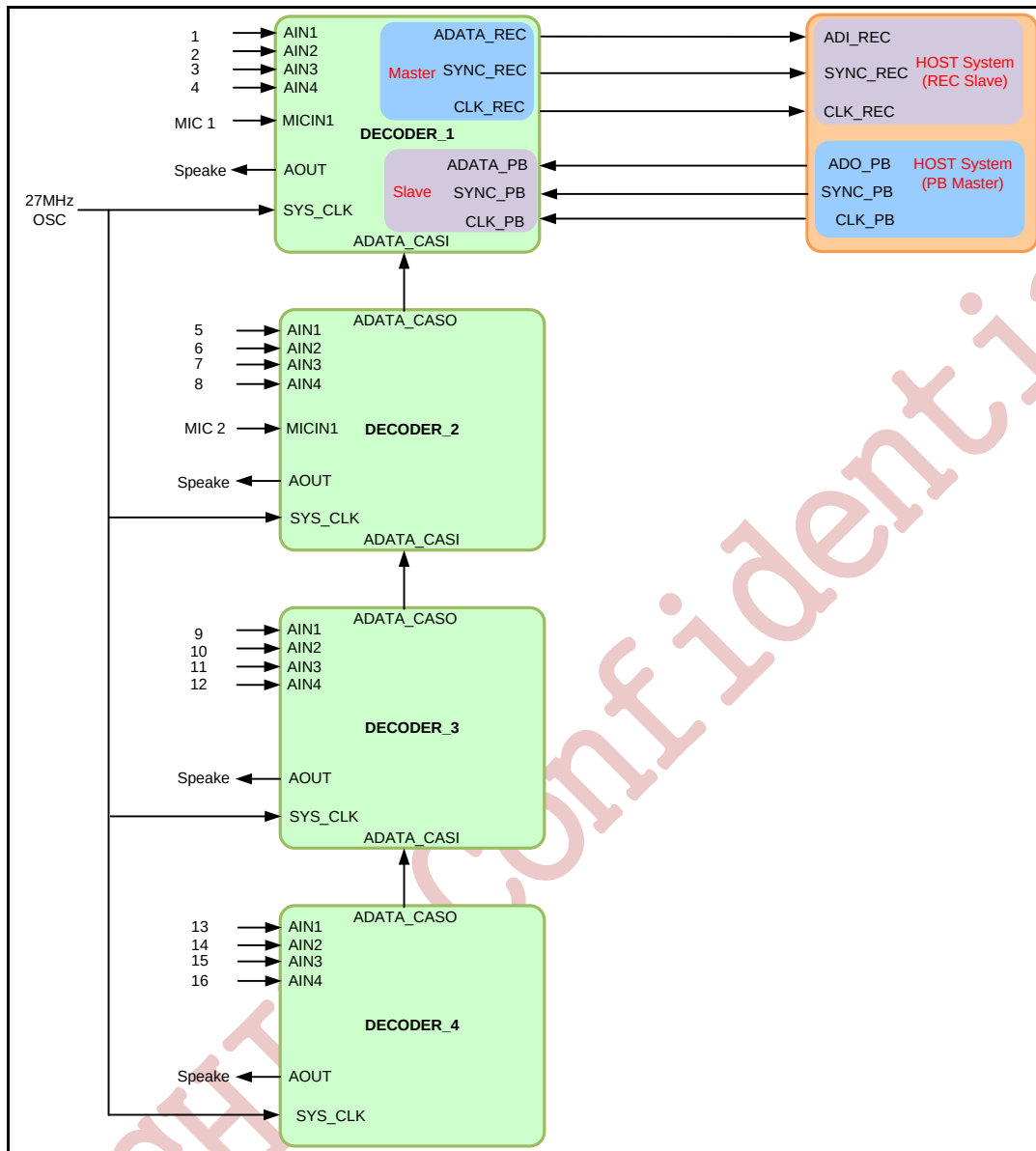


Figure 9.3 AUDIO 16-channel Mode

# Chapter 10

## PACKAGE INFORMATION

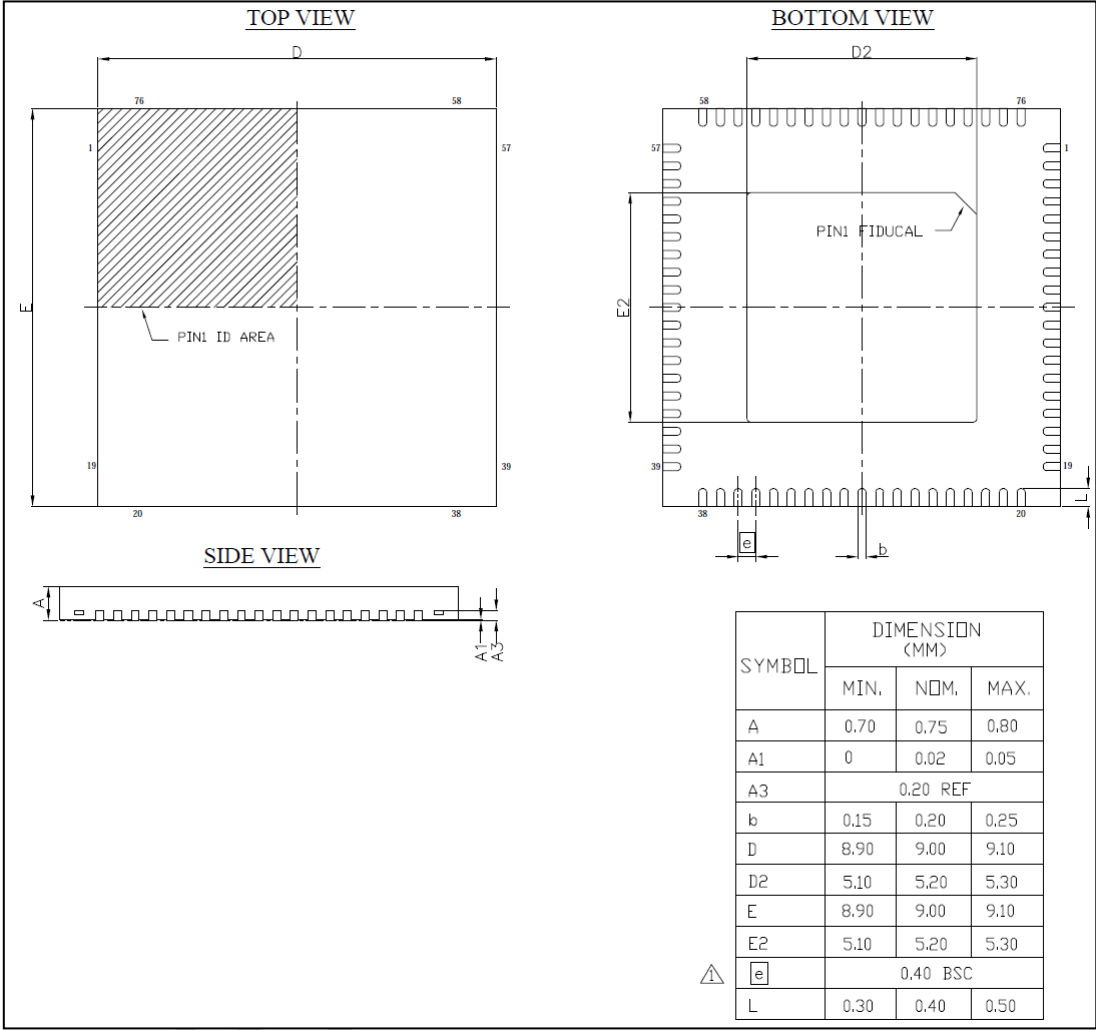


Figure 10.1 NVP6134C 76Pin Package Information